Textbook for Vocational Training – Components of Electrical Engineering/Electronics – Part 2

Table of Contents

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Preface

The present textbook is based on the rich experience of FRG vocational training and intended for trainees in the field of electrical engineering/electronics.

It contains the knowledge of electrical/electronic subassemblies/modules, the requirements imposed on them, the measuring processes on semiconductor units and explains the use of the subassemblies/modules in some selected basic circuits. Proceeding from basic knowledge of natural sciences and of electrical engineering and electronics, the necessary knowledge of this field of electrical engineering and electronics is presented in a didactically prepared form. Comprehensive illustrations and relevant tables as well as descriptive and comprehensible wording shall help the trainees to conceive the problems dealt with.

Considering the inseparability of theory and practice throughout, the textbook can be used by the trainees in both theoretical and practical vocational training.

The tasks and questions for recapitulation and testing at the end of the textbook concentrate on the main points of the necessary knowledge and shall help the trainees to examine the knowledge they have acquired.

1. Subassemblies/modules

1.1. Definitions and requirements

Any bigger device/equipment and all plants/installations are composed of parts. If such parts are able to perform a subfunction or serve a partial purpose, they are often called "functional units" or "subassemblies", respectively* The term "functional unit" features a circuitry fulfilling a specific function, such as voltage amplification. One or more functional units represent a constructional unit, a "subassembly". In this sense, "subassembly" is a generic term but, in practice, the two terms are also used as if synonymous in meaning.

Of special importance are functional units which are not designed for specific devices but can be used for many applications. Unification and thus a reduction of the variety of types can be achieved by adequate standardization. Power supply units, for example, can be centrally manufactured as subassemblies when the supply voltages of the equipment to be powered are limited to a few values only. Of course, it is necessary to graduate the available power but economic advantages remain, though, including, for example, specialization of the manufacturers. Specialization brings about an increase in productivity and improvement of quality. With an equipment consisting of subassemblies, any defective subassembly can be replaced in the event of failure. The down−time of the equipment is considerably reduced with a consequent increase in the up−time (availability). The defective subassemblies can be repaired by the manufacturer or in a specialized shop, again with higher productivity and better quality. Moreover, preliminary testing of subassemblies enables their reliability in service to be guaranteed which facilitates their assembling to produce a device, equipment, plant or installation.

These advantages have resulted in an ever increasing use of standardized subassemblies (modules) in so−called modular equipment or equipment of modular construction.

The development of functional units has been boosted by integrated circuits (IC). They themselves sometimes fulfill intricate functions of transmission and can be completed by a few additional components to a highly reliable functional unit. The functional units and subassemblies as well are named according to their function (amplifier, controller, rectifier), their purpose (power supply, coding, pulse generation) or location within the signal path (preamplifier, output amplifier). The use of functional units or subassemblies enables i.a.

– better standardization and, consequently, a reduction of the variety of types,

– centralized manufacture,

– higher reliability,

– easy replacement of the functional units/subassemblies and thus higher availability of the equipment using them.

1.2. Printed circuit boards (PCB)

1.2.1. Definitions and requirements

The printed circuit board is the base for printed circuits and includes the conductor tracks and all necessary holes. The printed circuit is a combination of a printed circuit board with components into an electrically functioning unit.

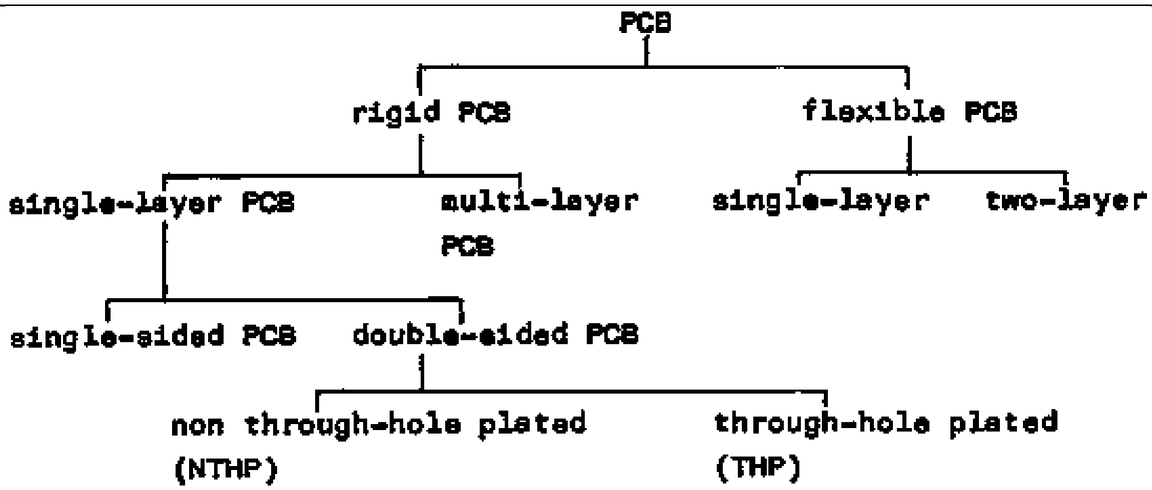


Table 1 Types of PCB

The construction of printed circuit boards is shown in the following illustrations:

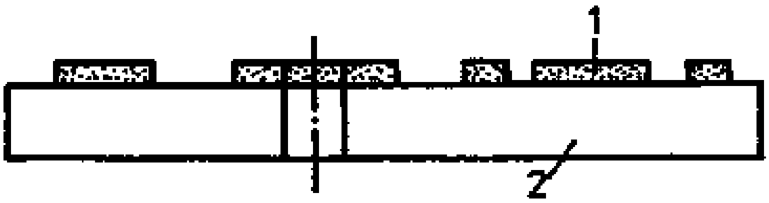


Figure 1 Single−sided PCB

1 conductor track, 2 base

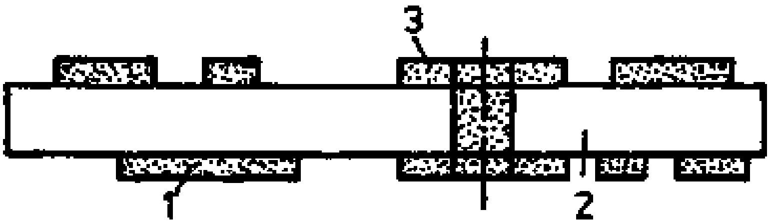


Figure 2 Two−sided PCB, through−hole plated (THP)

1 conductor track,
2 base,
3 through−hole

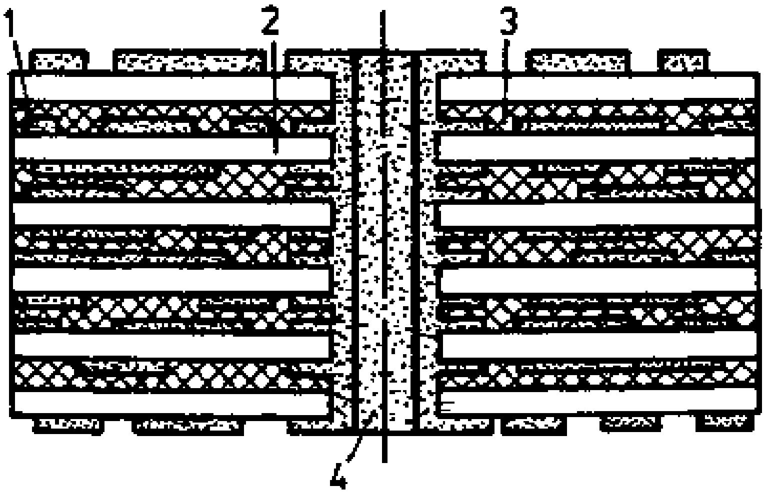


Figure 3 Multi−layer PCB

1 conductor track,
2 base,
3 intermediate layer,
4 metallized mounting hole

The base material for the manufacture of PC is an insulating material with or without bonded copper foil, "depending on the manufacturing method. Bonding of the copper foil is also called coating or cladding or laminating. The base material must be resistant to heat, flux and washing agents and feature dimensional stability and adequate electric properties. The thickness of copper foil is 25/µm, 35/µm and 70/µm. The base materials used include:

Laminated paper (Pertinax)

Laminated paper (hard paper) is a laminate of cellulose paper sheets with phenolic resin as bonding agent. it is produced in copper−clad boards of various nominal thicknesses. It is mostly used for single−sided PCB (copper−clad at one side).

Epoxy glass−laminated fabric

Epoxy glass−laminated fabric is a laminate of glass silk fabric with epoxy resin as bonding agent.

It is used for two−sided and multi−layer PCB (copper−clad on two sides).

Because of better properties, epoxy glass−laminated fabric should be preferred to laminated paper.

Polyester foil

Polyester foil is used for flexible PCB.

The imagined graticule of two groups of equidistant parallels crossing at right angles, with holes for mounting the component connections located in the crossing points, is called "base grid". Rigid component connections correspond to the reference grid. The base grid is required for standardized PCB design. The reference base grid is the size for the distance of two adjacent lines of the base grid (2.5 mm).

The secondary grid is the finer subdivision of the base grid (for NTHP 0.5 or 1.25 mm, for THP 0.5 mm). At present the manufacture of PCB features four levels of difficulty. The level of difficulty determines the method necessary for the PCB manufacture.

The classification of the levels of difficulty is based on the following criteria:

– hole spacing,
– extent of soldering,
– conductor track width,
– conductor track spacing,
– conductor track pattern,
– type of connectors.

The levels of difficulty are standardized.

1.2.2. Assembly of PCB

Placing of adequately prepared components on a component carrier (PCB) including subsequent fixing is called assembly (or insertion) of PCB.

The assembly method may be

– manual or
– automatic.

The assembly process includes several steps which can be combined, depending on the assembly method applied.

<u>Components</u>

The component connections are designed in accordance with the standards and requirements of two−dimensional conductor patterns.

Types of components:

– discrete components,
– integrated circuits,
– printed components.

Discrete components are parts having a basic electric function (capacitor, resistor, diode, etc.).

The connections are pointed soldering lugs, soldering pins or wires. The connections have a length of at least 1.5 to 3 mm from the component side of the PCB.

Heavy components have auxiliary mechanical connections. The distances between rigid connections must correspond to the standard reference grid of the PCB.

The following criteria are important for mounting:

– Components with axial connections at both ends are directly placed on the base board with the connections to be angled.

The components should rest on the board. Otherwise the soldering lug on the conductor side can be lifted off the base material together with the conductor track when pressure is exerted on the soldered component.

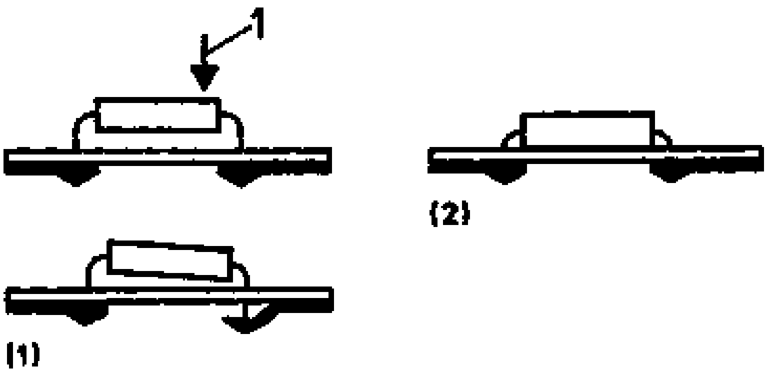


Figure 4 Mounting of components

(1) wrong
(2) correct
1 pressure

– Components with connections at one end can be placed on the PCB in erect position (space–saving).

– Components specifically designed for PCB have connection ends to suit the assembly process.

Integrated circuits are microelectronic components where all or some of the circuit elements on the surface or within the volume of a base body are permanently interconnected.

In spite of different electric designs of the circuits, the bodies of their components have a standard geometric configuration. This facilitates the assembly expenditure, handling and magazining for an automated assembly process. The connections comply with the standard reference grid (2.5 or 1.25 mm grid). The multitude of connections calls for high precision of the component connections and PCB holes.

Printed components are directly integrated in and printed together with the conductor pattern, e.g. connectors, switches, inductors, capacitors.

Component preparation means finishing the components in a way best suited to assembling and bonding. Such preparation considerably increases the working speed of the manual assembly process. Component preparation includes finishing of the component connections, such as

– bending to reference grid,
– cutting to size,
– beading for the snap–in technology (see Fig. 11).

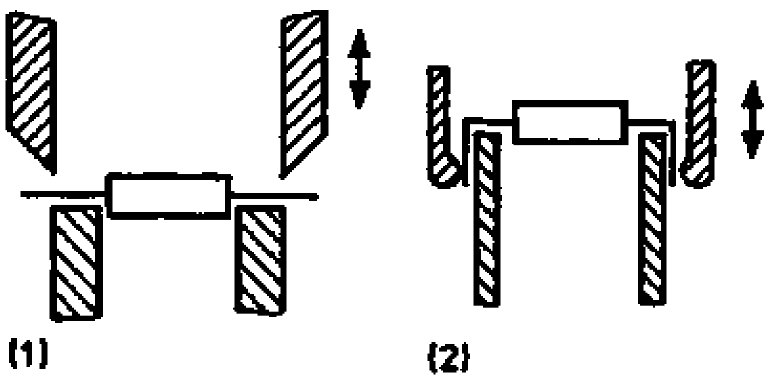


Figure 5 Finishing of connecting wires

(1) cutting,
(2) bending

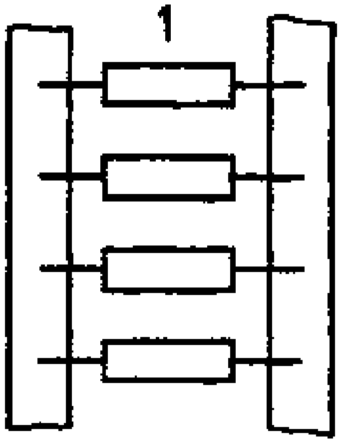


Figure 6 Taped components

1 tape

Cutting and bending devices are used for quicker working of the component connections. Taped components (sticking on adhesive tapes) or non–taped components can be handled (Fig. 6). Bending and cutting sizes are adjustable. Automatic machines handling taped components have a considerably higher working speed since the individual components need not be loaded into the devices.

Manual assembly

The components are manually inserted or placed. Advantages:

– Constant visual inspection of the PCB and of the assembly process.

– Any arrangement of the components on the PCB and any size and type of PCB are possible.

Disadvantages:

– Long assembly time.
– Wrong assembly is possible but can be largely reduced by assembling aids.

In the manual assembly without assembling aids, prepared component connections are bent with round or flat nose pliers and inserted in the PCB holes.

The components should be preferably inserted so as to leave the marking visible (advantage in the event of repairs!). The connections are to be cut so as to project by about 1.5 mm on the conductor track side.

Connection ends must not be cut off after soldering since the side cutting plier exerts tensile forces on the wire (which might destroy the intermetallic bond between solder and connecting wire produced by soldering).

With series assembly the prepared components are made available in marked bowls. The PCB is held in partly swivelling assembly frames.

The assembly is based on

– a drawing showing the parts or the complete component side,
– the component print on the PCB or
– a PCB sample.

The most critical operation in the manual assembly with assembling aids is the insertion of the components. This is manually done, while handling and control are largely automatic. The advantages are reduced assembly times and reduced reject rate.

Assembling aids are:

Indication of the mounting holes (by illumination of the mounting holes from beneath or, by projection, from above).

Release of the appropriate component (by interlocking and by light signal).

In order to prevent displacement of the inserted components prior to the subsequent soldering operation, the components are to be fixed. This can be done in various ways:

Straight−line component connections:

Before and during the soldering process the components are pressed on the PCB with a pad of foamed material.

Figure 7 Straight−line connections

The connection ends are bent at right angles.

Figure 8 Connections bent at right−angles

This necessitates that sufficient soldering lugs are available.

The wires are to be bent only in the direction of the respective track to prevent a reduction of the conductor distance or short circuits by projecting wires.

Unsoldering in the event of repairs, however, is difficult.

− The connection ends are bent at an angle of 20 to 30 degrees. The consequent high friction in the inside wall of the PCB hole prevents the component from falling out.

Figure 9 Connections bent at angles of 20 to 30 degrees

− The connection ends are crimped so that their diameters are bigger than the hole diameters.

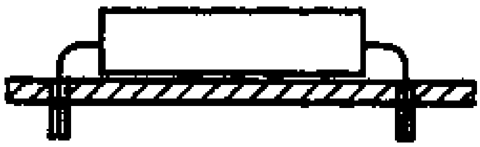


Figure 10 Crimped connections

− The components are provided with shaped connections (snap−in technology).

Figure 11 Shaped connections

− The cone−shaped connections are firmly inserted in the hole (frictional connection).

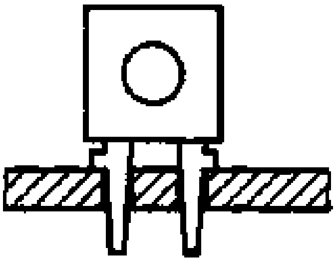


Figure 12 Cone−shaped frictional connections

– Integrated modular components of dual−in−line (DIL) type are just plugged in. The modular component is held in the hole by the friction of the angled connections.

The maximum bending angle of OIL modules is 15 degrees.

– Connections of integrated modular components of flat pack type cannot be plugged in but are placed on the bonding surfaces of the PCB and are then soldered or welded onto it. Fixing of the modular component is only possible by adhesives.

Since flat pack modular components cannot be used for mass−production soldering, they should be bonded as soon as possible after the assembly.

Automatic assembly

In addition to automatic handling, automatic assembly also includes automatic positioning and insertion. The PCB to be automatically assembled, however, must have clamping surfaces and location holes for the positioning device of the machine. Insertion machines perform all finishing operations and the assembly process. They are equipped with:

– Magazine
to make available the components to be assembled, e.g.

• roller magazine for taped components (for components with axial connections),
• fall shaft magazine for integrated modular components.

– Insertion head
to receive the component from the magazine, align and cut the connections and insert the connections into the PCB holes.

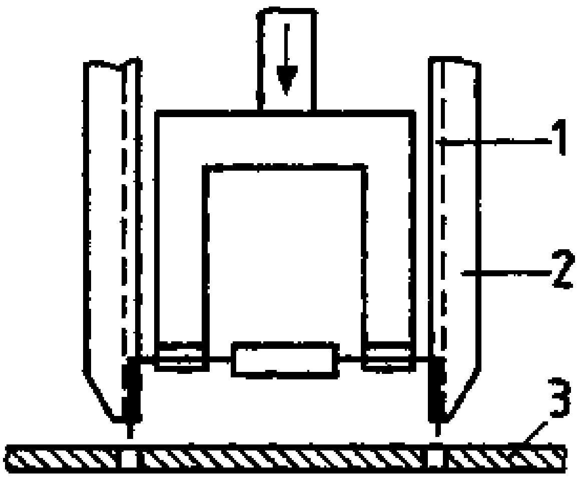


Figure 13 Schematic of insertion head

1 guide slot,
2 guide rail,
3 PCB

– Positioning device
to locate the PCB and set the exact position of the mounting holes under the insertion head

(minimum tolerances admissible only).

– Control system
to control the selection of the magazines, the positioning and materials handling operations.

Further rationalization of the assembly process can be achieved by:

– insertion machines linked up into transfer lines including materials handling facilities

– insertion machines working to the pantograph principle to enable several components to be inserted on the PCB (complete assembly of the PCB is possible)

– insertion machines equipped with a greater number of magazines and controlled by data carriers.

When insertion machines are used, it is to be made sure that they are continuously utilized. Moreover, insertion machines call for precisely manufactured PCB and components.

1.2.3. Soldering of PCB

After insertion of the components, the connections of the components are to be connected with the conductor track by soldering.

PCB can be soldered manually or automatically (soldering bath method).

The PCB and components are subjected to heavy thermal stress during soldering. Therefore the selection of the correct soldering parameters (temperature and time) is important to proper soldering.

The solderability of the PCB and of the component connections dictates the lower limit for temperature and time. Maximum load in terms of temperature and time is limited by the soldering resistance of the component parts which depends on the PCB type used and precludes less resistant component parts from use for the subassembly.

Soldering requirements:

– Components may be soldered and unsoldered if admitted by their solderability and soldering resistance.

– First soldering of multi–layer PCB is to be performed on machines.

– Any PCB must resist soldering for at least three times and unsoldering for at least two times without functional damage.

Functional damage means, for example:

– defective connection,

– defective insulation,

– conductor track lift–off,

– soldering eye lift–off (In repair soldering, soldering eye lift–off on the component side is considered a functional damage only if the soldering eyes are connected to conductor tracks.),

– increased delamination (inclusion of air and faulty bonding in the base material),

– roundabout cracks in the hole metallization.

Table 2 Maximum soldering parameters

	Manual soldering		Machine soldering	
	temperature deg.C	time s	temperature deg.C	time s
Laminated paper	280+20	3	250+5	5
Epoxy glass−laminated fabric ELL	280+20	3	250+5	8
MLL (initial machine soldering only)	320+10	6	250+5	8
polyester	230	2	225+5	2

The maximum soldering parameters of the components to be soldered (e.g. semiconductor components) are also to be taken into account for soldering.

Manual soldering

Manual soldering is applied for single and group soldering operations. The soldering device mostly used is the soldering iron.

Best suited to manual soldering is multiple flux cored solder, such as hollow wire 2SW32, LSn60 or LSn50. It is available in various wire diameters (1.0, 1.2, 1.5, 2.0 and 3.0 mm). With flux cored solder it is not absolutely necessary to use flux, otherwise acid/free flux or pure rosin are recommended. For soldering, the bit of the soldering iron is to be held for a short time to the component connection above or at the soldering eye, at the same time applying the solder to the heated soldering point. The solder must flow uniformly around the component connection on the soldering eye. Through−hole plated mounting holes must be through−soldered up to the component side.

Maximum soldering parameters are to be observed!

Bonding methods for flexible PCB are: soldering with soldering iron, bow−type soldering, wave soldering, welding, plug−bonding and screw−bonding. The method mostly used is soldering with soldering iron.

Defects that may occur by bit temperatures of 280 to 400 degrees C when using soldering irons without temperature control:

– Lift of conductor tracks off the polyester fool.
– Warping of the foil,
– Melting of the foil in the soldering eye area.
(Therefore it is necessary to use temperature−controlled soldering irons.)

Favourable soldering parameters:

– Soldering temperature: 230 degrees C
– Soldering time: 1...2 seconds
– Copper bit, axially bored (tubular)
– LSn60 solder.

The oxide solvency of rosin flux is not sufficient for the soldering temperature of 230 degrees C. Therefore, it is necessary to use flux with activating additives (if necessary, washing of the soldering point).

Note:

Instead of a temperature−controlled soldering iron, a 220 V soldering iron with undervoltage (140...160 V to achieve the soldering temperature of 230 degrees C) can be used.

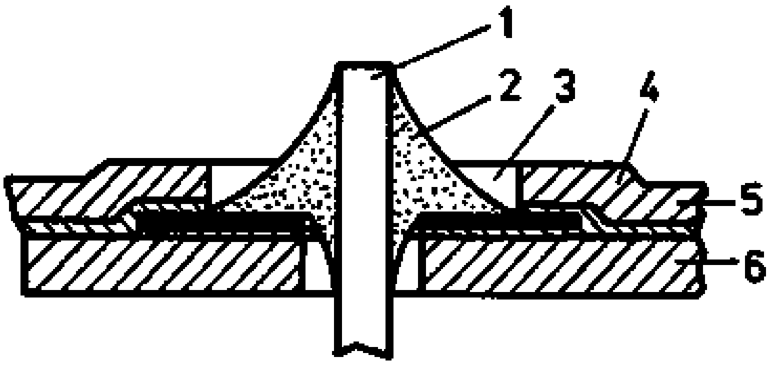


Figure 14 Sectional view of a soldered joint on a flexible PCB

1 component connection,
2 solder,
3 soldering eye,
4 polyurethane adhesive,
5 covering polyester foil,
6 polyester foil (base foil)

Bath soldering

Most efficient method of bonding big quantities of plug−in components with PCB.

Conditions for bath soldering:

− The PCB must have only one component side.

− The opposite side (soldering side) is to be used for bonding only.

− All component connections must protrude from the mounting holes by at least 1 mm and not more than 3 mm.

− Equal solderability of all connections must be guaranteed (prior test, if necessary).

With bath soldering, the soldering side of the PCB is dipped into molten solder. In this way the solder required for bonding and the thermal energy necessary for soldering are taken from the soldering bath.

The soldering bath is electrically heated and temperature−stabilized (+/−2 degrees C).

The PCB must be prepared for bath soldering by

− placing a solder resist (mask),
− applying of flux,
− preheating.

The solder mask consist of paper resist or liquid resist (varnish) and is placed on the conductor tracks prior to insertion of components and bathing, respectively, so as to solder the soldering eyes of the PCB only (selective soldering).

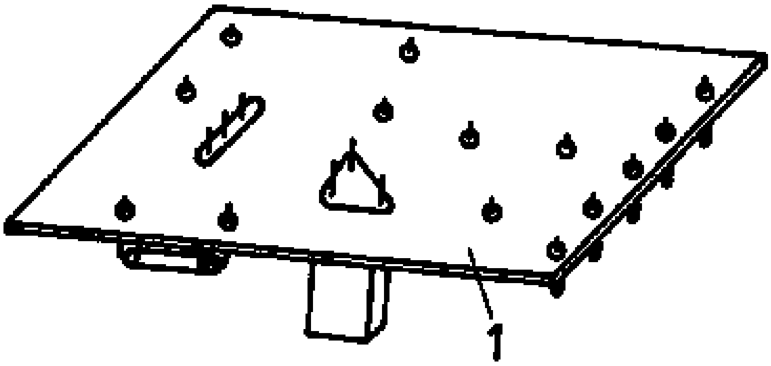


Figure 15 Solder mask

1 paper or liquid resist

Advantages of the solder mask are

– solder savings,

– low thermal stress of the PCB,

– prevention of solder bridging between adjacent conductor tracks,

– protection of finished metal surfaces on the soldering side of the PCB (e.g. plug contacts).

Applying of flux on the entire PCB is by

– flux−coated rotating rolls,

– spray nozzles,

– dipping of the soldering side of the PCB into stagnant flux or into a flux wave (wave fluxing),

– touching a foam wave produced at the flux surface by compressed air (foam fluxing).

Flux is to be applied thinly only!

Preheating serves for drying of the flux.

Temperature: 50 to 80 degrees C. The solvents are removed so as to avoid detrimental effects by vapour on the soldering process. Preparing the PCB for the soldering temperature shall avoid a thermal shock.

There are two ways of bath soldering: dip soldering and wave (or flow) soldering.

Dip soldering

All connections are soldered at the same time by dipping into a soldering bath at a temperature of 220 to 270 degrees C. The surface of the soldering bath is stagnant.

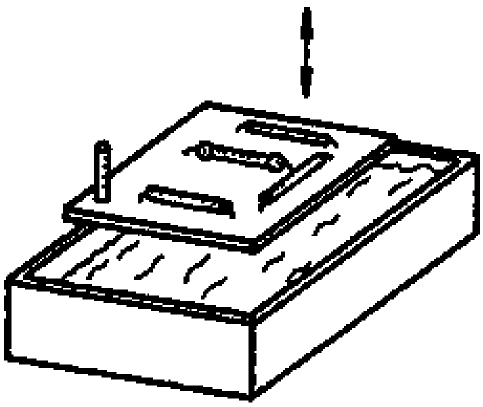


Figure 16 Schematic of dip soldering

Dip−soldering methods:

– Vertical dip soldering
The PCB is vertically dipped into the soldering bath surface. Difficulty escaping flux vapours and a lot of sticking solder may result in soldering defects.

– Angular dip soldering
The PCB is dipped at an angle, set vertically and then lifted at an angle again. Vapours can escape, less solder at the soldering points.

– Drag soldering
The PCB is dipped at an angle and dragged horizontally over the bath. Dragging and lifting

speeds are normally adjustable to achieve the optimum soldering pattern. No solder bridging or solder fins.

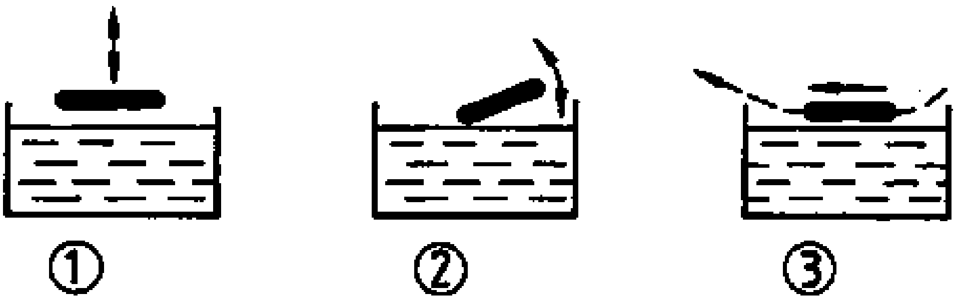


Figure 17 Dip−soldering methods

1 vertical dip soldering,
2 angular dip soldering,
3 drag soldering

The soldering temperature normally is 240+/−5 degrees C with different soldering times between 1 and 8 seconds, depending on the PCB type.

The oxide film forming on the surface of the bath is to be mechanically removed by a wiper prior to any dipping.

Wave (or flow) soldering

Wave soldering is the method mostly applied in the manufacture of subassemblies. The soldering bath surface rises locally in the form of a wave. The PCB is moved horizontally or at a small angle through the crest of a solder wave. Advantages of wave soldering:

− No impurities on the surface of the wave because of permanent movement.
− PCB is subjected to low thermal stress.
− Conductor patterns with high level of difficulty can be soldered.

Disadvantages of wave soldering:

− Wave−soldering equipment is more expensive.

− More vigorous oxidation of tin because of permanent movement of the bath (possibly oil cover or permanent filtering of oxide).

− Bath contains more solder.

The wave is generated by pumping the solder via a feed channel through a wave nozzle. The opening of the wave nozzle has the form of a slot the width of which is adjustable (adjustability of different wave forms). The PCB is moved at right angles to the slot and in opposite direction to the movement of the wave. The speed of the PCB movement is adjustable to achieve the optimum soldering time.

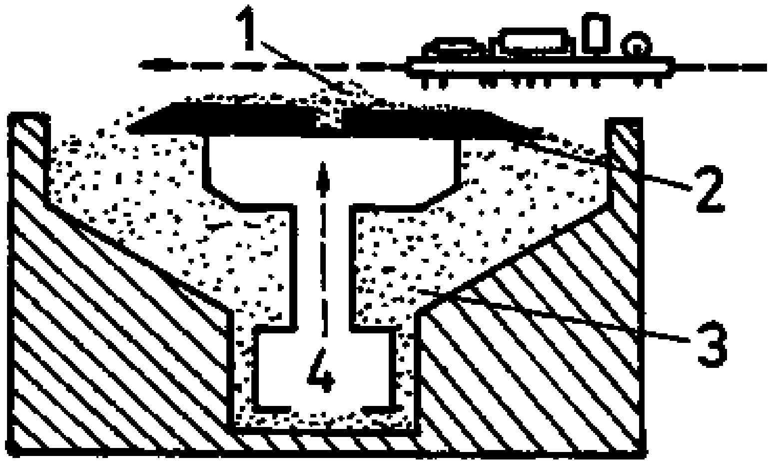


Figure 18 Schematic of wave soldering

1 wave,
2 slide valve to adjust the slot width,
3 solder,
4 pumps

Special one−off soldering methods

− Soldering with bow−type electrode.
− Soldering by heat radiation.

Infrared beams or light beams of halogen quartz lamps are I focused on the soldering point and converted into heat (light−beam soldering) or gases are burnt off in close vicinity to the soldering point with smallest flame (microflame soldering).

1.3. Power supply unit

1.3.1. Definitions and requirements

Any equipment and almost any functional unit need to be powered by energy to fulfill their functions. Electrical functional units are appropriately supplied with electric energy from the electric network (mains). The subassembly preparing such energy in the form required and making it available is called "power supply unit". The required form may refer to

− D.C. or A.C. energy,
− voltage or amperage,
− necessary power (wattage),
− admissible ripple,
− tolerance and stability of voltage or amperage,
− no potential or potential to earth.

Modern equipment and plants use semiconductor components to a great extent. They require only low working voltages which are normally not dangerous to life. Therefore, repair or maintenance work is often done in working order.

The power supply unit is almost permanently under mains voltage. Any work done on it in working order is dangerous to life!

Therefore it is better to get used to working on dead equipment or subassemblies. If this is not possible, e.g. in fault finding, it is absolutely necessary to comply with the safety requirements.

For any work on power supply units it is important to make sure that they are disconnected from the mains and that the safety regulations are observed.

1.3.2. Rectifiers

In many cases D.C. voltage is required for the operation of plants or equipment* For this purpose, the A.C. voltage made available by mains transformers is to be rectified. The functional unit "rectifier" uses components acting like valves, normally semiconductor diodes.

Depending on the power and admissible ripple, the circuits are of single−phase, two−phase or three−phase (sometimes also of polyphase) type using only one half−wave (single−pulse circuit) or the two half−waves of an A.C. oscillation (two−pulse circuit), They are also called half−wave (or single−way) rectifiers and full−wave (or double−way) rectifiers.

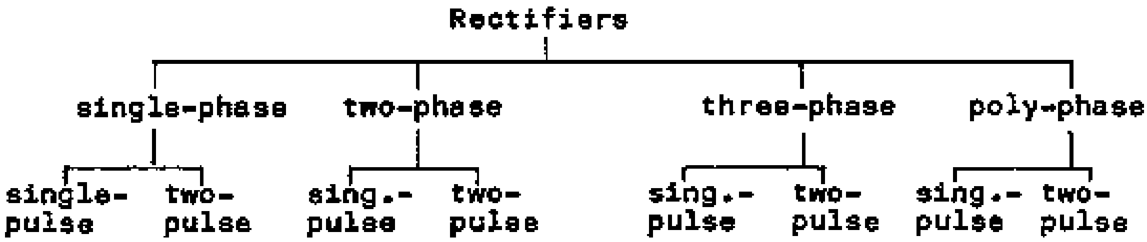


Table 3 Types of rectifiers

Single−phase single−pulse rectifiers

This simple circuit utilizes just one half−wave for rectification.

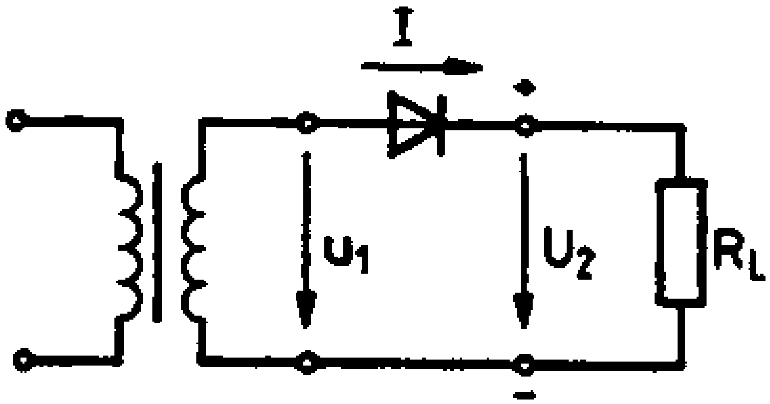


Figure 19 Single−phase single−pulse rectifier circuit

The voltage at the consumer, therefore, is a heavily pulsating direct voltage resulting in an equally pulsating direct current.

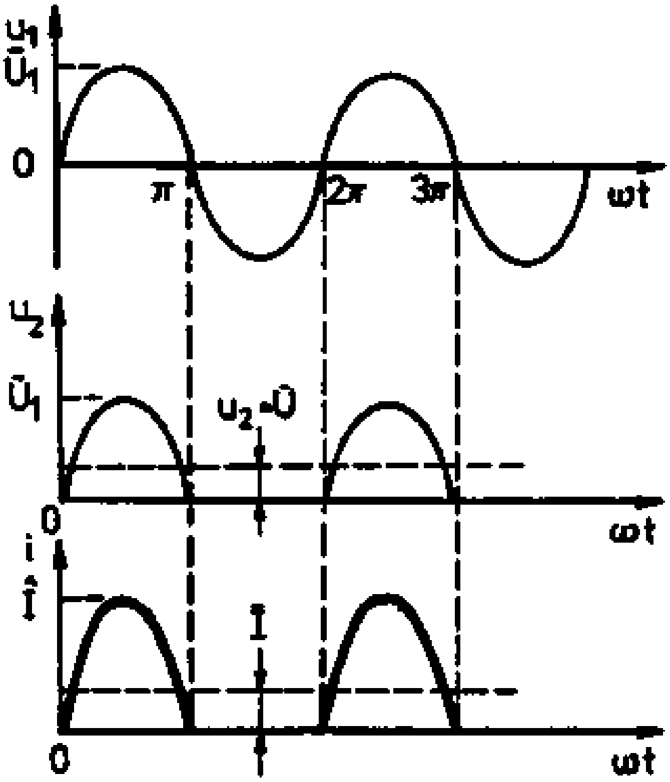


Figure 20 Voltage and current behaviour in a single−phase single−pulse rectifier circuit with ohmic load

The average voltage (arithmetic mean) for sinusoidal unput (alternating) voltages is

$$\overline{U}_2 = U_= = \frac{\hat{U}_1}{\pi} = 0.318 \cdot \hat{U}_1 = 0.45 U_1$$

U_1 effective A.C. voltage or for the current intensity

$$\bar{I} = \frac{\hat{I}}{\pi} = 0.318 \cdot \hat{I} = 0.45 \cdot I.$$

In addition to the heavy pulsation of the direct voltage and direct current, there are still other disadvantages:

− The transformer winding is passed−through by a (pulsating) direct current which premagnetizes the core.

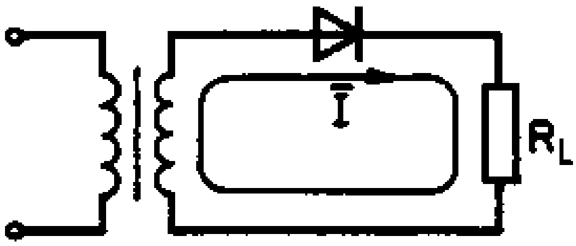


Figure 21 Direct−current flow through the transformer winding

− Heavy ripple "w" which is defined as the ratio of the alternating voltage portion (effective value) to the direct voltage portion after rectification.

$$w = \frac{U_\sim}{U_=}$$

Therefore, this circuit configuration is applied only for low powers (P less than 0.5 kW).

With inductive consumers the ratios are considerably improved when a diode (zero diode) is connected in parallel. The diode permits a current to flow even at the end of the positive alternating voltage half−wave. From 0 to ? there flows the current I_1 which is driven by the transformer voltage.

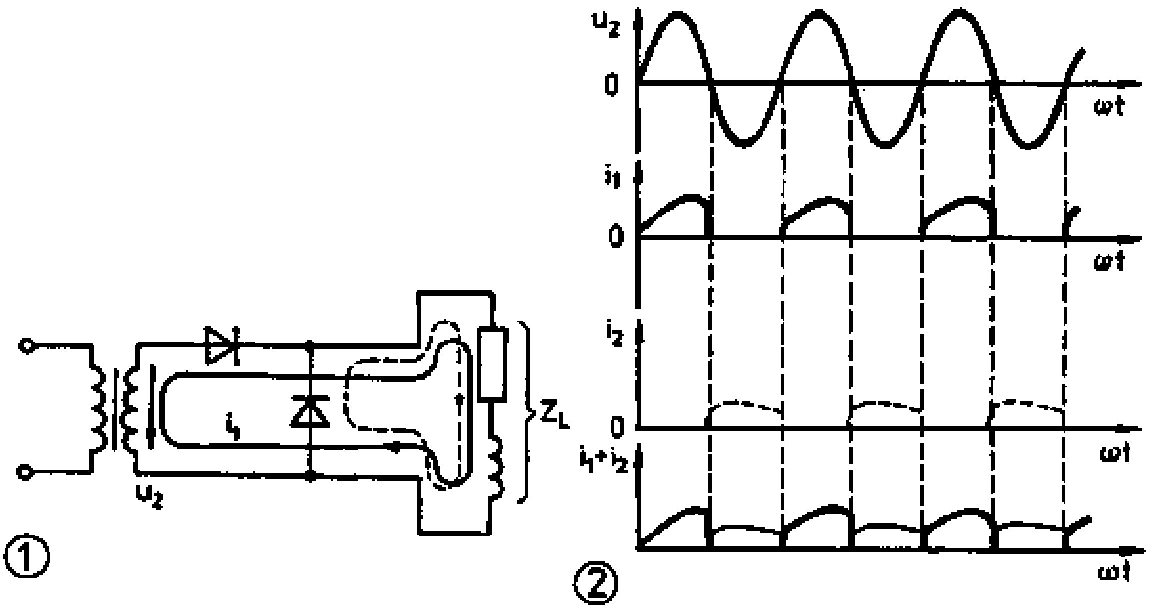


Figure 22 Direct−current flows with the use of a zero diode

1 type of connection,
2 voltage and current behaviour in the connection

From ? to 2 ? there flows the current I_2 which is driven by the energy stored in the consumer inductance.

Single−phase two−pulse rectifiers

This circuit is also called "bridge circuit" or "diamond circuit".

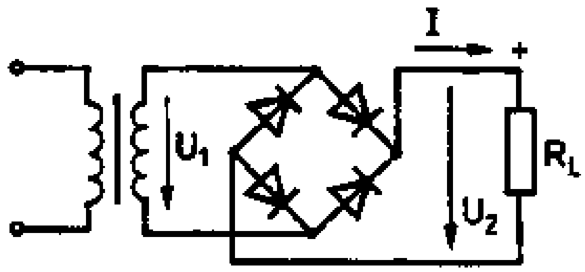


Figure 23 Single−phase two−pulse rectifier circuit

The two half−waves are utilized, the direct voltage portion

generated is bigger. For sinusoidal alternating voltages and ohmic consumers this is reflected by

$$\overline{U}_2 = U_= = \frac{2_{\hat{U}1}}{\pi} = 0.636 \cdot \hat{U}_1 = 0.9 \cdot U_1$$

The time cycles are shown in Figure 24 (2). Figure 24(1) makes clear that the diodes are conductive in one half−wave each and the currents sum up at the consumer (load resistance). Since the current flow cyclically gets zero here, too, because of the consumer, the ratios for inductive consumers can also be improved by the use of a zero diode. Compared to the single−pulse circuit, there is less ripple.

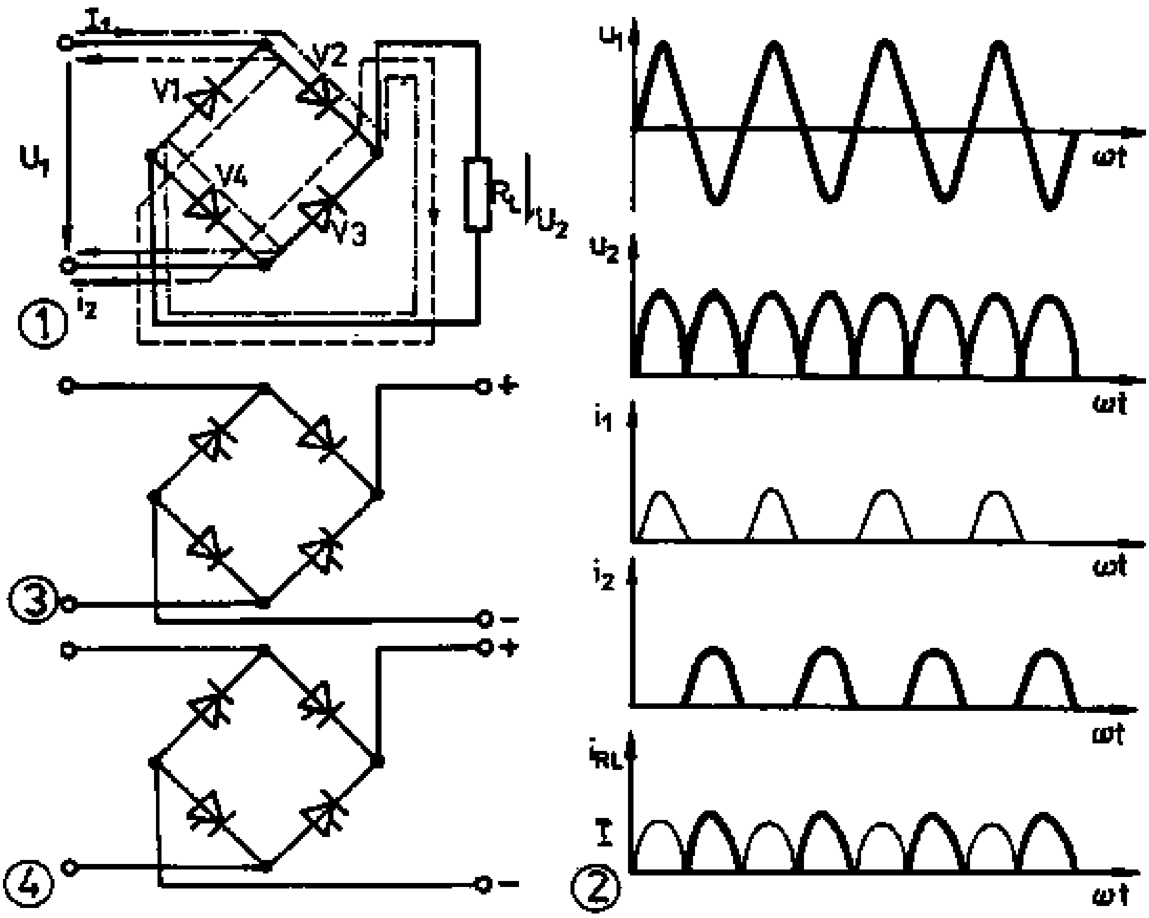


Figure 24 Single−phase two−pulse rectifier

1 type connection,
2 voltage and current behaviour with ohmic load.
3 semi−controlled bridge circuit,
4 fully controlled bridge circuit

When two or all four diodes are replaced by thyristors, the direct voltage U_2 can be controlled by them (semi−controlled or fully controlled bridge circuit, Figure 24 (3) and 24 (4)). Single−phase bridge circuits are used up to powers of P = 5 kW.

Two−phase single−pulse rectifiers

This circuit is also known as "centre tap connection". Compared to the bridge circuit, a more expensive transformer is required since two equal secondary windings are necessary for the generation of the voltages in phase opposition. Since this circuit has equal properties but no advantages, the bridge circuit is preferred.

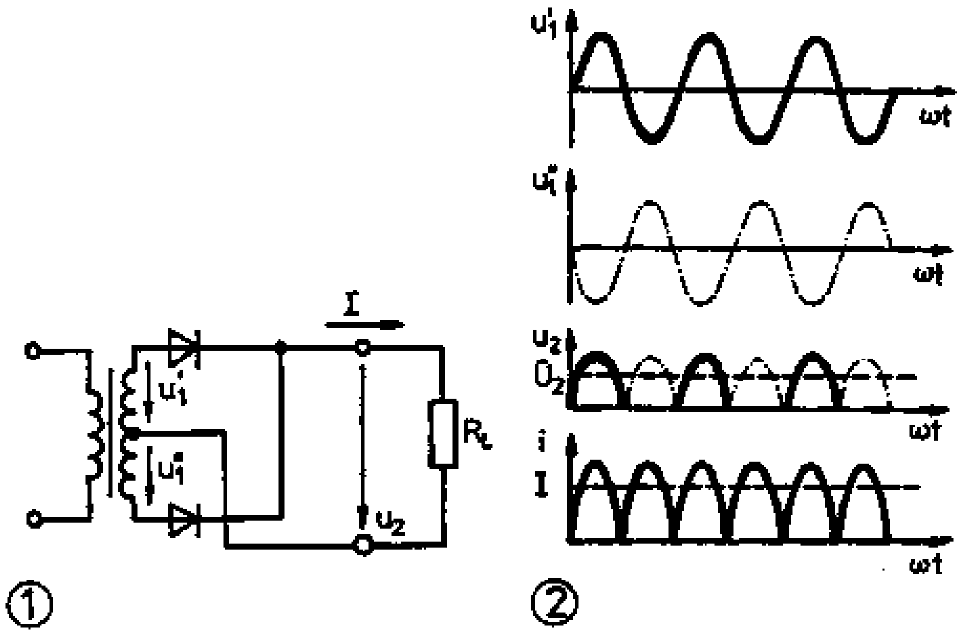


Figure 25 Two−phase single−pulse circuit

1 type of connection,
2 time behaviour of current and voltage

<u>Three−phase single−pulse rectifiers</u>

With three−phase feeding, there is considerably reduced ripple because more and more half−waves are used for the generation of the direct voltage. Since the individual phase powers sum up, three−phase rectifiers are also suitable for high powers. The output voltage of the three−phase single−pulse rectifier is

$$\overline{U}_2 = U_= = 1.17 \cdot U_1$$

The three−phase single−pulse circuit is used for lower powers only because the transformer is also passed through by direct current.

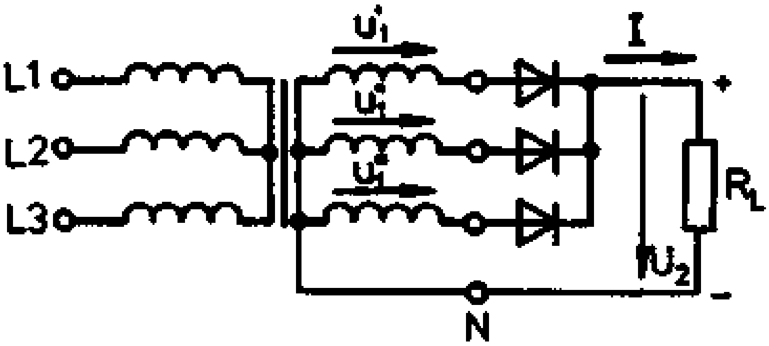


Figure 26 Three−phase single−pulse rectifier circuit

<u>Two−phase two−pulse rectifiers</u>

This possible combination is hardly used in practice since there are no or but a few linked two−phase systems and the benefit would not justify the expenditure for creating an internal, linked two−phase voltage in an equipment.

<u>Three−phase two−pulse rectifiers</u>

The utilization of the two half−waves further reduces the ripple and increases the direct voltage to:

$$\overline{U}_2 = U_= = 2.34 \cdot U_1$$

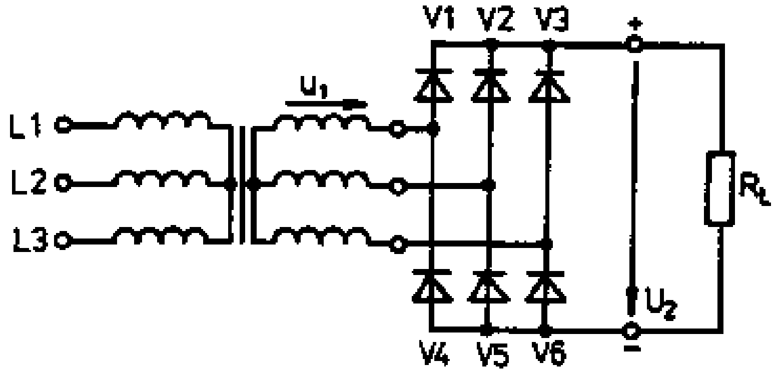


Figure 27 Three−phase two−pulse rectifier circuit

This circuit, also called "three−phase bridge circuit", can be applied for powers of up to several megawatts. Figure 28 shows how the voltage Up is composed of the individual half−waves. In this circuit, too, three diodes (V_1...V_3) or all six diodes can be replaced by thyristors. This will result in semi−controlled or fully controlled three−phase bridge rectifiers which enable the output voltage to be controlled.

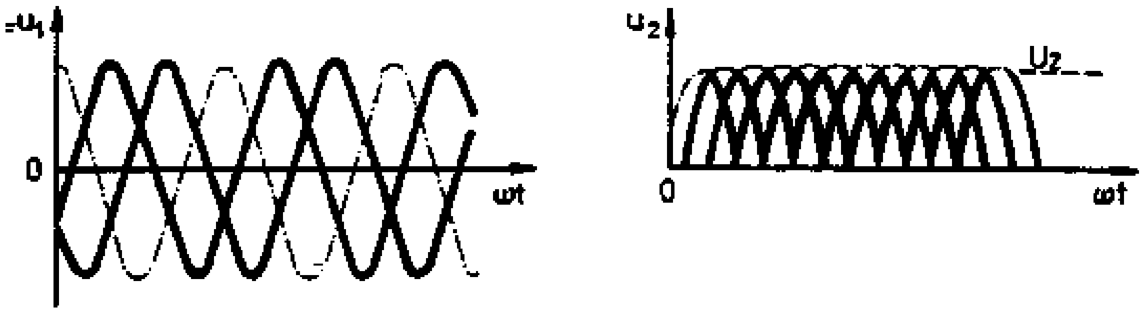


Figure 28 Voltage behaviour in a three−phase bridge circuit with ohmic load

1.3.3. Voltage doublers

In some cases higher direct voltage is required than that available as supply voltage. Direct voltages cannot be directly transformed. If considerably higher direct voltages are required, the transverter principle is applied. This provides for conversion of the direct voltage into a pulse by an electronical chopper, followed by upward transformation and subsequent rectification. According to the energy conservation law:

$P_1 = P_2 + P_v$	P_1 power input
$U_1I_1 = U_2I_2 + P_v$.	P_2 power output
	P_v power loss

Because of the inevitable power the following applies:

The power output is always less than the power input ($P_2<P_1$).

The general connection diagram shown in Figure 29 is based on the transverter principle with "n" being possible for any transformation ratio but depending only on the selected transformation ratio of the transformer (not shown in the illustration).

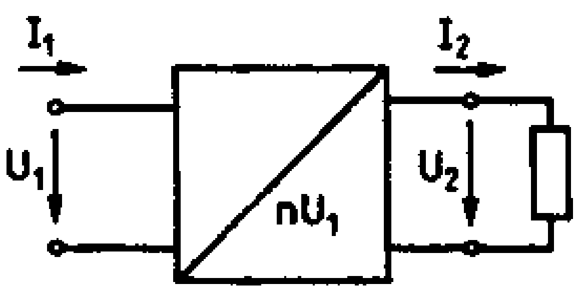


Figure 29 Energy relations in a voltage multiplication circuit

If the supply voltage is an alternating voltage (output voltage of a transformer), doubling is relatively easy. For this purpose the rectifier circuit is extended. For better understanding, the effect of a connected capacitor shall be considered first.

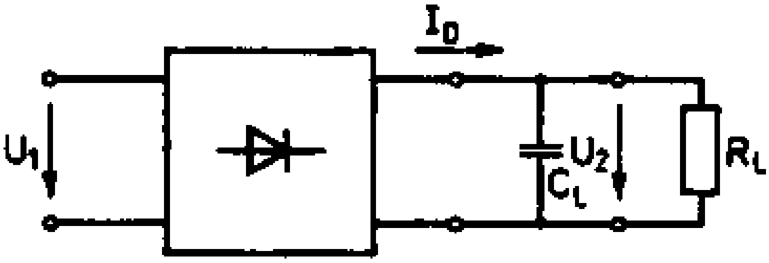


Figure 30 Rectifier circuit with charging capacitor

With all rectifier circuits the form of the output voltage changes considerably when a capacitor C (charging capacitor) is switched on. The time behaviour is shown in a simplistic I representation in Figure 31.

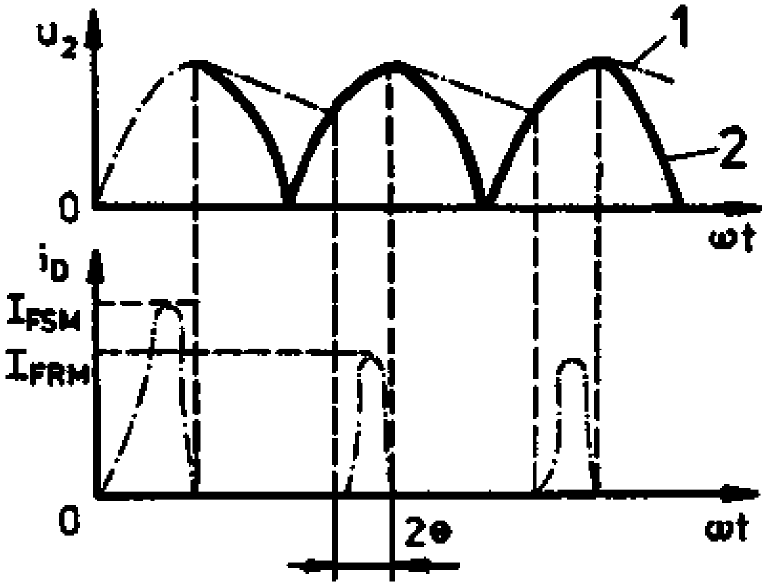


Figure 31 Voltage and current behaviour in a rectifier circuit with charging capacitor (simplified)

1 with C_L
2 without C_L

The effects of a charging capacitor in a single−phase single−pulse circuit are shown in Figure 32.

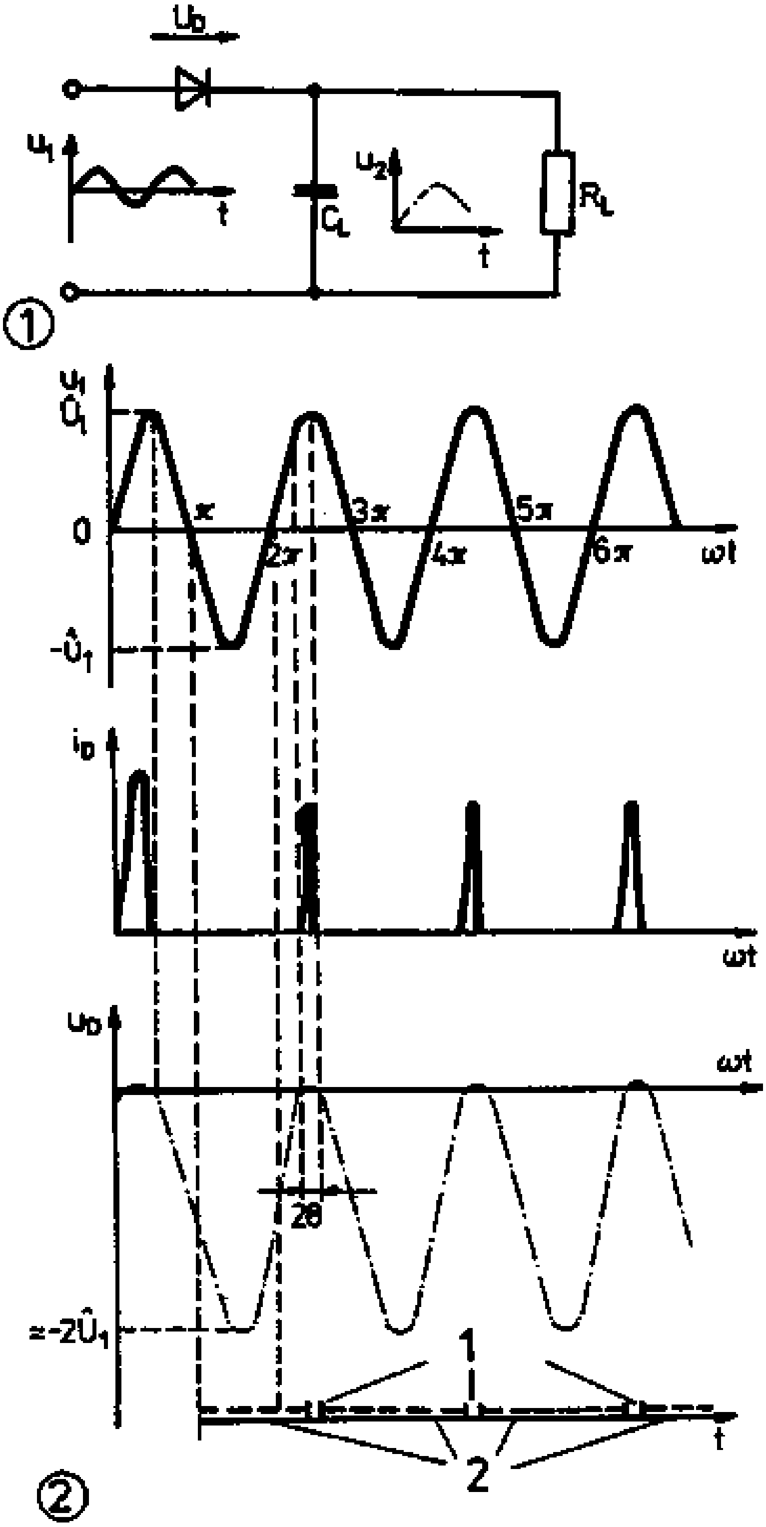


Figure 32 Voltage relations in the diode of a single−phase single−pulse circuit

(1) type of connection
(2) voltage behaviour
1 diode conductive
2 diode blocking

The preconditions are as follows:

A current flow through a diode is possible only when the potenitial at the cathode is more negative than that at the anode. Assuming that the capacitor C_2 is discharged when switching on, C_L is charged in the first half−wave (0 ? ?t = ? / 2). The intensity of the flowing current must not exceed I_{FSM}. When the voltage is decreasing again after ?t =?/2, the diode is blocking because its anode potential is lower than the cathode potential retained by C_L In the blocking stage of the diode, C_L starts discharging through R_L. When with the next positive half−wave the diode's anode potential again gets higher than its cathode potential, which is equal to the instantaneous voltage through C_L, the diode becomes conductive again and C_L is again charged to the peak value of the alternating voltage. The time necessary for this corresponds to double the angle of current flow (H). Consequently, the current, the intensity of which must not exceed the periodic on−state current I_{FRM}, is flowing through the diode only for a short time. Because of the storage effect of the capacitor, the voltage load of the diode increases. In the blocking stage, with existing capacitor, the diode features a partial voltage $U_{RRM} \approx 2\hat{U}_1$. The diode must be designed accordingly. With entirely ohmic load, the blocking load of the diode is reduced to $U_{RRM} \approx \hat{U}_1$ (Fig. 32 (2)) because electric energy is not stored with an ohmic resistance. The advantage of less ripple with the use of a charging capacitor is achieved at the expense of higher voltage load of the diode.

The remaining ripple, which is also called hum or ripple voltage U_{Br}, is approximately

$$U_{Br} = K \cdot \frac{I = max}{C_L}$$

$I_=$ = max. output D.C.
K = 3.18 (two−pulse circuits)
K = 6.36 (single−pulse circuits).

U_{Br}	$I_{=max}$	C_L
V	mA	µF

The storage effect is also utilized in doubler circuits. Figure 33 shows the cascaded circuit and the Greinacher circuit

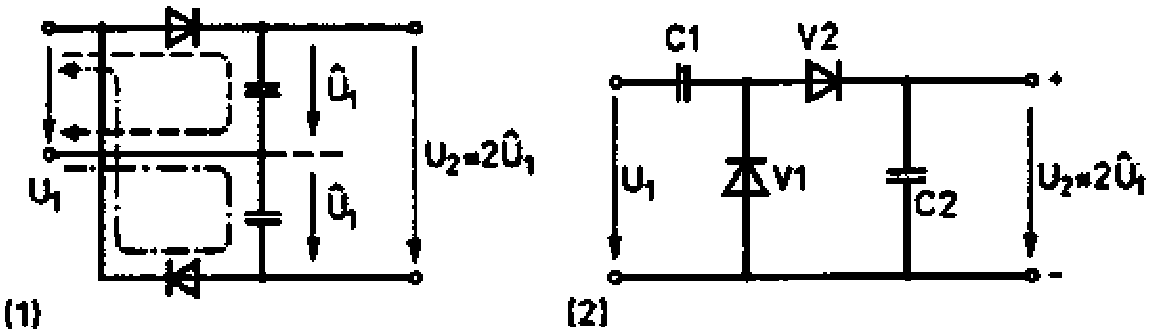


Figure 33 Voltage−doubling circuits

(1) cascaded circuit,
(2) Greinacher circuit

The Greinacher circuit is composed of two series−connected single−phase rectifiers one of which utilizes the positive and the other one the negative half−wave.

The situation with the cascaded circuit is more intricate. Therefore, Figure 34 separately shows the current flows in the two half−waves of the energizing alternating voltage.

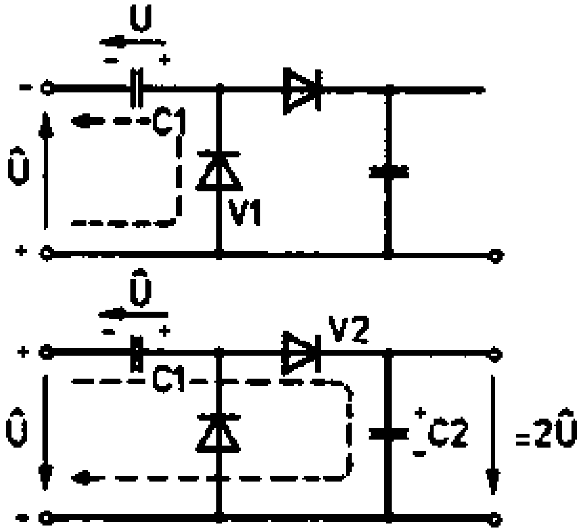


Figure 34 Effect of voltage doubling in a cascaded circuit

In the negative half−wave V1 is conductive and C1 is charged with the polarity shown in Figure 34; in the positive half−wave V1 is blocking. The voltage through C1 is in series with the supply voltage. V2 becomes conductive and C2 is charged with the sum of these two voltages. A connected load discharges the capacitors, the output voltage gets lower. Therefore high capacitances are to be used.

1.3.4. Filtering units

When the voltage supplied by the rectifier circuit is used for feeding of electronic circuits, there is too much ripple even with the use of a charging capacitor. Often a few millivolts of ripple voltage only are admissible for analogue amplifiers. Therefore, the A.C. portion remaining after rectification is to be suppressed by a suitable circuit. This function is performed by the functional unit "filtering unit".

A filtering unit must transmit the D.C. energy with the least possible attenuation and suppress (dampen) the A.C. energy to the maximum possible extent.

<u>Resistance−capacitance filtering unit</u>

Figure 35 shows the use of an additional resistor (filter resistor) and of an additional capacitor (filter capacitor) in a rectifier circuit. With this circuit, the transmission of the D.C. energy is heavily damped when the resistance R_S gets too high.

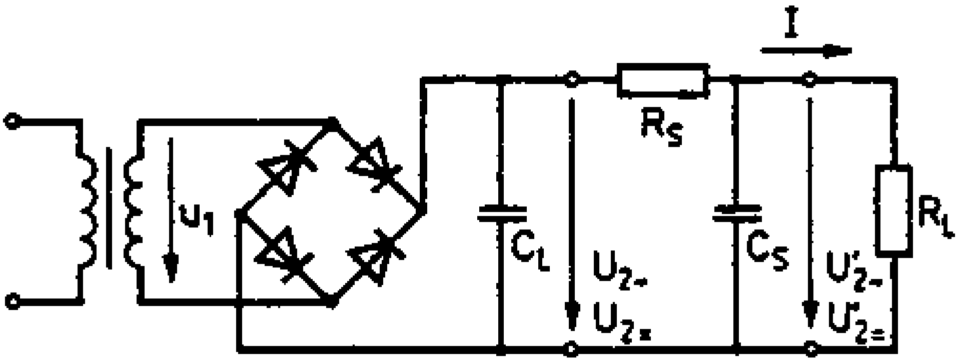


Figure 35 Resistance−capacitance filtering unit

Figure 36 shows the filtering unit as voltage divider the ratio of division of which becomes dependent on the frequency by the filter capacitor C_S. For direct voltages the capacitor represents a very high resistance.

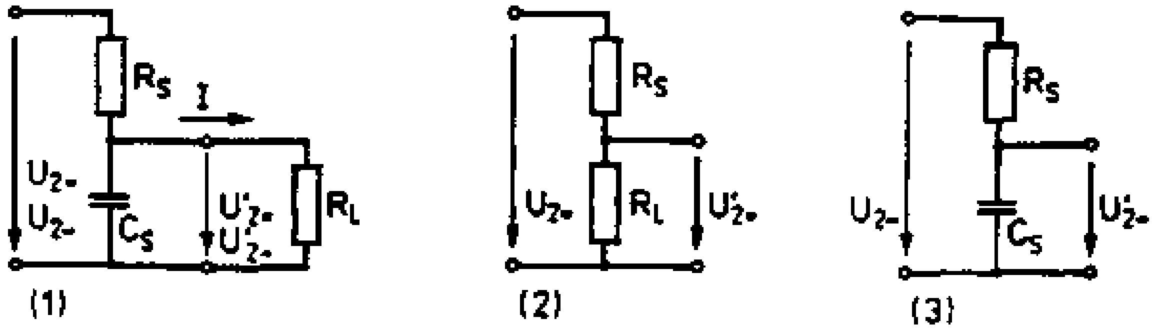


Figure 36 Resistance−capacitance filtering unit as frequency−dependent voltage divider

(1) complete,
(2) for direct voltage,
(3) for alternating voltage

Direct voltage at the load resistance R_L:

$$U_2^{'} = U_{2=} \frac{R_L}{R_L + R_S} = U_{2=} \frac{1}{1 + \frac{R_S}{R_L}}$$

$U_{2=}$' is approximately $U_{2=}$ only if

$$\frac{R_2}{R_L} << 1, \text{i.e.} R_S << R_L.$$

Alternating voltage:

$$U_{2\sim}^{'} = U_{2\sim} \frac{\frac{1}{\omega C_S}}{\sqrt{R^2 S + \left(\frac{1}{\omega_S C_S}\right)^2}} = U_{2\sim} \frac{1}{\sqrt{1 + (\omega_S C_S R_S)^2}}$$

The reciprocal value of this ratio of voltage division is called "reciprocal of reduction factor":

$$S = \left|\frac{U_{2\sim}}{U_{2\sim}^{'}}\right| = \left|\sqrt{1 + (\quad {}_S D_S R_S)^2}\right|$$

Normally applies: (? $_S C_S R_S)^2$ >>1, and then

S ? ?$_S C_S R_S$

?$_S$ = 2? f_s

f_s is the frequency effective for filtering of the ripple voltage and depends on the number of phases and pulses of the various rectifier circuits.

$f_s = m\ n\ f_N$

m number of phases
n number of pulses
f_N mains frequency (50 Hz).

More effective suppression of the ripple voltage is possible in three−phase rectification because f_S is higher than in single−phase circuits. The reciprocal of reduction factor is becoming higher.

Choice–capacitance filtering unit

The use of a choke (Fig. 37) instead of a filter resistor brings about the following advantages:

– low D.C. resistance ($R_s = R_{Cu}$),
– high A.C. resistance (X_s = ?$_s$ L_S).

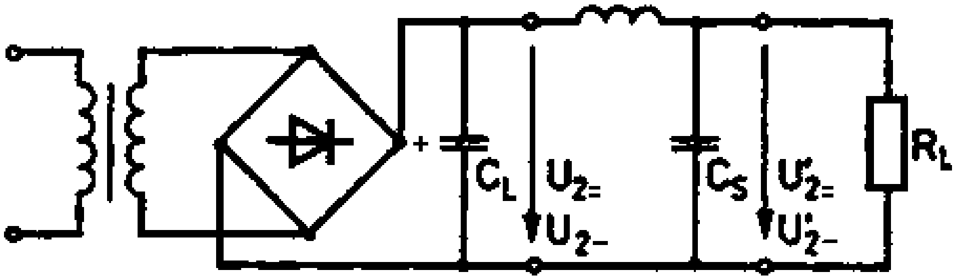


Figure 37 Rectifier circuit with charging capacitor and choke–capacitance filtering unit

This results in little damping of the D.C. portion and heavy damping of the A.C. portion. The reciprocal of reduction factor

$$S = \left|\frac{U_{2-}}{U'_{2-}}\right| = \left|\frac{\frac{1}{\omega_S C_S} + \omega_S L_S}{\frac{1}{\omega_S C_S}}\right| = \left|1 - \omega_S^2 L_S C_S\right|$$

The curve of the reciprocal of reduction factor in dependence on ?$_S$ is shown in Figure 38.

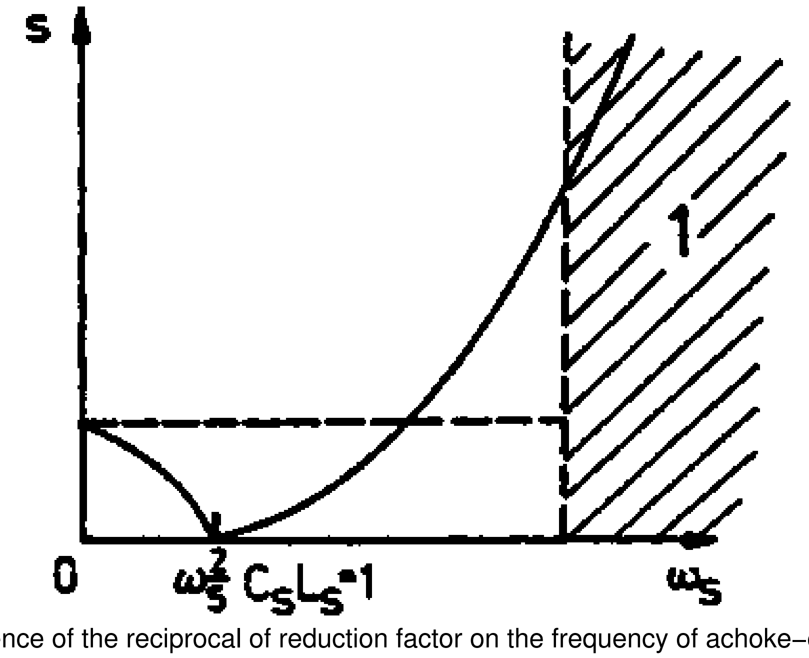


Figure 38 Dependence of the reciprocal of reduction factor on the frequency of achoke–capacitance filtering unit

1 working range

S >> 1 calls for ?$_s^2$ $L_S C_S$ >> 1; therefore, calculations can mostly be based on

S ? ?$_S^2$ $L_S C_S$

1.3.5. Voltage stabilizers

If the voltage needs to be constant over a longer time, it is necessary to stabilize it. Depending on the degree of stabilization required, very simple but also very intricate functional units are available for this purpose. Normally simple circuits will do for power supply of subassemblies.

The quality of stabilization is represented by the stabilization factor:

$$S = \frac{\frac{\Delta U_1}{U_1}}{\frac{\Delta U_2}{U_2}} = \frac{\Delta U_1}{U_2} \cdot \frac{U_2}{U_1}$$

U_1 input voltage
?U_1 input voltage change
U_2 output voltage
?U_2 output voltage change.

<u>Z–diode stabilizers</u>

The Z–diode characteristic is ideal for voltage stabilization. In a relatively wide current range there is but little change of the (avalanche) voltage. This characteristic range is utilized.

Figure 39 shows the basic circuit. In practice U_2 is always known; it is equal to the voltage U_z of the Z–diode and has the value of the required voltage to be stabilized. The load resistance R_L and, consequently, the load current I, may vary. The same applies to the input voltage U_1.

The practical problem is to calculate the resistance R_V so as to guarantee stabilization and prevent overloading of the Z–diode.

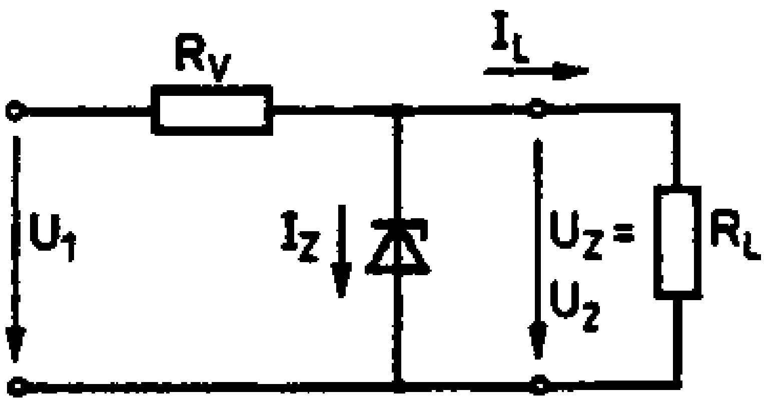


Figure 39 Voltage stabilization with Z–diode

Since, for manufacturing reasons, the avalanche voltage of the Z–diode, also varies around an average value, stabilization is possible only on certain conditions.

Such conditions are:

– With minimum input voltage and maximum load current, the diode current must not be lower than the lower limit value I_{Zmin}.

U_{1min} ? $(I_{Lmax} + I_{Zmin})\ R_v + U_{Zmax}$

– With maximum input voltage and minimum load current, the diode I current must not exceed the upper limit value I_{Zmax}

U_{1max} ? $(I_{Lmin} + I_{Zmax})\ R_v + U_{Zmin}$

Thus two limit values are to be taken into account for the calculation of the resistance R.

$$R_v \le \frac{U_{1min} - U_{Zmax}}{I_{Lmax} + I_{Zmin}} \cdot \frac{1}{1+p}$$

$$R_v \ge \frac{U_{1max} - I_{Zmin}}{I_{Lmin} + I_{max}} \cdot \frac{1}{1-p}$$

p stands for the selected tolerance of the value of the series resistor.

<u>Transistor stabilizers</u>

If the stabilization factor achieved by the simple Z–diode circuit is not sufficient or if the efficiency factor is not acceptable, the use of transistors can bring about considerable improvements. Normally one transistor is connected in series before the consumer as adjustable resistance. The resistance is adjusted through a circuit so as to keep the output voltage (voltage at the consumer) constant.

In practice, this type is called "longitudinally controlled stabilization".

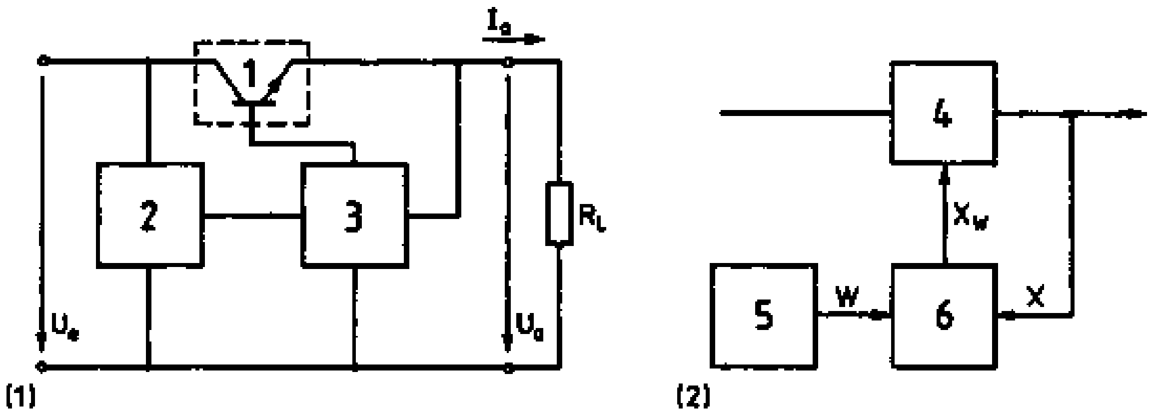


Figure 40 Longitudinal controlled voltage stabilization

(1) general drawing,
(2) representation as closed–loop control circuit
1 control transistor,
2 reference voltage,
3 comparator,
4 actuator,
5 reference valve,
6 controller

Figure 40 (2) shows a closed–loop circuit configuration. The control transistor must carry the total load current and resist the voltage difference $U_e - U_a$. This load may be of tremendous amount. A Z–diode can be used for reference voltage supply. Its voltage is compared with the output voltage in a comparator. In the event of any deviation, the resistance of the control transistor is adjusted so as to regain the desired (output) voltage. The calculation of the stabilization factor is more difficult. Values of S ? 10^2 ...10^4 can be achieved, depending on the level of sophistication. In practice, the simpliest way to determine S is by measuring the output voltage change. A simple longitudinally controlled voltage stabilization circuit is shown in Figure 41. It offers the advantage of overload protection. The available current intensities and the stabilized voltage depend, to a great extent, on the transistor V1 and on the Z–diode voltage (V3). U_a can be adjusted by R5.

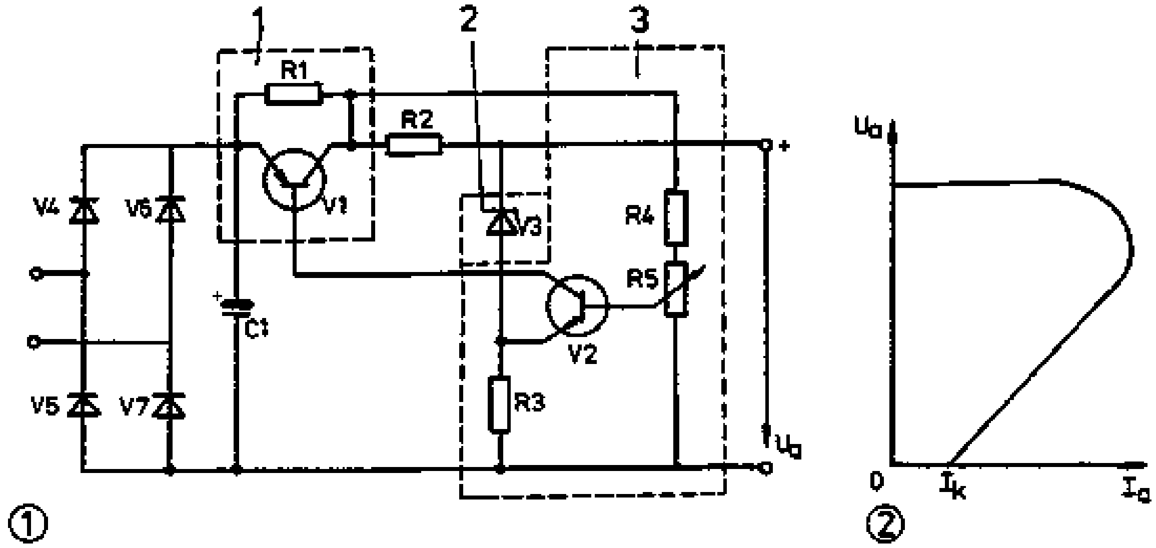


Figure 41 Short−resistant longitudinally controlled voltage stabilization circuit

(1) circuit diagram,
(2) output characteristic
I_K short−circuit current
1 control transistor,
2 reference voltage,
3 comparator

Prior to the explanation of the stabilizing effect, some basic connections shall be clarified. The partial voltage over the Z−diode V3 is to be considered constant. Any change of the output voltage U_a, therefore, fully appears at the resistor R3 and thus at the emitter of V2 while it is damped at the base of V2 by the voltage divider R4 − R5. Thus the base emitter voltage at the transitor V2 decreases with increasing output voltage. The collector current intensity of V2 decreases and thus the intensity of the base current of V1 as well. The control transistor V1 is less highly controlled, it becomes more highly resistive and the output voltage drops because V1 is acting like a dropping (adjustable) resistor. The chain of cause and effect is represented by:

$$U_e \uparrow \rightarrow U_a \uparrow \rightarrow U_{R3} \uparrow \rightarrow (I_C)_{V2} \downarrow \rightarrow (I_B)_{V1} \downarrow \rightarrow (U_{CE})_{V1} \uparrow \rightarrow U_a \downarrow$$

In the event of overload or short circuit, the output current intensity is heavily increasing. Thereby the control transistor is overloaded or destroyed unless such overloading is prevented by protective measures (switching off or current limitation to a harmless value).

In the circuit as per Figure 41 the output voltage U_a is decreasing with increasing output current intensity because of the increased partial voltage I_aR2. The Z−diode starts blocking and U_{R3} is reduced. But the voltage of the Z−diode is the reference voltage (for comparison) of the stabilizer. The transistor V2 tries to reduce the output voltage because it is comparing it with the lower reference voltage. This is possible only by additional control of the control transistor V1. This results in a further drop of U_a. A state of equilibrium is achieved which depends on the load at the output. In the event of short circuit at the output, V1 is nearly blocked and the current intensity limited to a harmless value. The effect of current intensity limitation is shown in Figure 41 (2) by the output characteristic,

Integrated circuit stabilizers

The circuitry "can be considerably simplified by the use of integrated constant−voltage controllers.

[The integrated constant−voltage controllers available for standard voltages look like power transistors, i.e. they have only three connections.

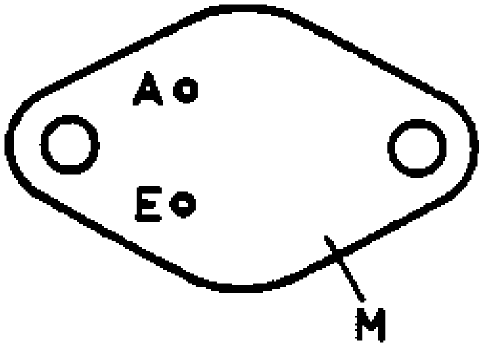


Figure 42 Integrated constant−voltage controller

M mass, E input, A output

The use of such controllers further reduces the component expenditure. Adequate internal circuitry makes such types short−circuit−proof, insensitive to thermal overload and protected against second breakdown − some of the advantages of microelectronics.

With all longitudinally controlled stabilization circuits the energy losses are relatively high, the efficiency is about 40%. The considerable heating of the longitudinal or control transistors connected with this necessitates good cooling. Energy losses must be minimized!

1.3.6. Switching power supply units

Switching power supply units are more and more used for power supply in order to reduce the high energy losses. The basic principale is shown in Figure 43.

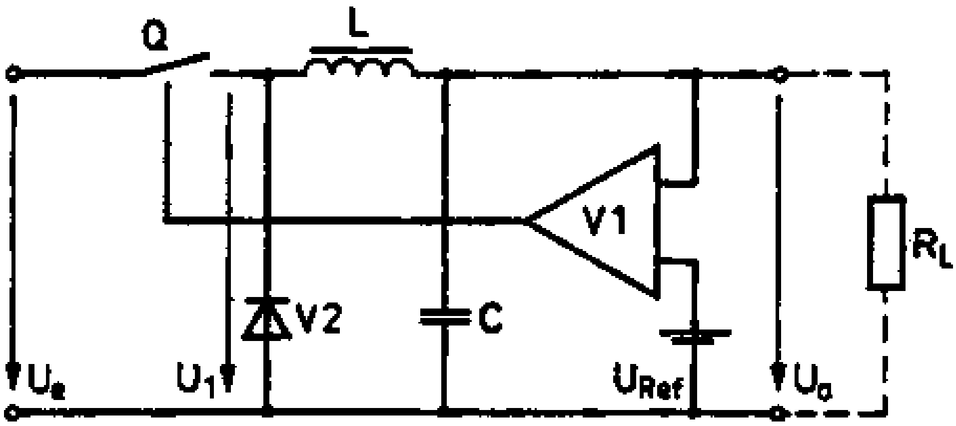


Figure 43 Schematic of switching power supply unit

The comparator V1 closes the switch Q when the output voltage U_a becomes lower than the reference voltage U_{Ref}, it opens when U_a is higher than U_{Ref}. When the switch is closed, the capacitor C is charged and a magnetic field built up in the coil L.

When the switch is open, the energy stored in this magnetic field is reduced by a current flow through the consumer and the diode V2, i.e. it is converted at the consumer into active energy. Thereby the efficiency is improved to about 70% but the output voltage is more rippled than in the case of longitudinally controlled voltage stabilizers.

The switches used are transistor switches which enable considerably higher switching frequencies than mechanical switches. The values achieved in practical applications are about some kilohertz. The basic voltage curves are shown in Figure 44.

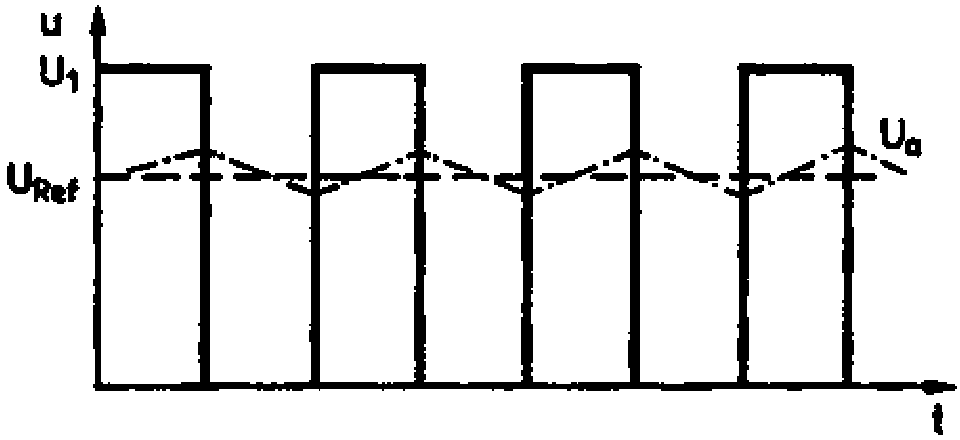


Figure 44 Voltage behaviour in a switching power supply unit

The coil manufacture is difficult because the coil must have an inductance of some millihenrys even with higher direct currents, otherwise it cannot store sufficient energy.

In spite of that problem, switching power supply units are increasingly used for power supply because with the development of high−blocking transistors the power transformer is not necessary any longer and microelectronic driver circuits can be used for such transistors.

It is specially to be mentioned that then there is no voltaic isolation from the power supply system.

Disconnection from the power supply system (isolating transformer) is absolutely necessary for any work on electrical circuits!

1.4. Analogue circuits

1.4.1. Definitions and requirements

Almost all data determining a process are analogue signals* Such signals can be further processed in their analogue form or transformed into the digital form by means of a converter. The method of further processing of signals in their analogue form is widely used.

All circuits, which do such further processing, are called analogue circuits. The entire complex, in general, is called also "analogue technology".

Since, however, analogue signals between two limit values may assume any intermediate value, disturbances are to be particularly minded when further processing such signals. The disturbances arising right in the circuit are of particular interest. Such disturbances may be caused by noise, hum voltages, drift phenomena and inductively or capacitively coupled interference voltages. These disturbances distort the signals which is particularly obtrusive in such instances where the amplitude of the value to be transmitted serves as measure for the signal, so to say as signal parameter. To reduce the effects of the disturbances on the analogue signal, A−D conversions are made to an increasing extent. This requires, however, a considerable technological effort which, in turn, hampers the quick introduction and wide use of such conversion. Since the signals from a process have often to be amplified and are analogue in their original form, analogue circuits, specifically amplifiers, will continue to be widely employed also in the future.

1.4.2. Amplifiers

The signal energy generated from a process value does often not suffice to feed secondary evaluation equipment, i.e. a servo unit.

In such event, the energy is to be intensified or amplified. The functional unit doing this job is called amplifier.

The amplification v signifies the ratio between the output value and the input value of a signal.

In the event of this ratio being smaller than 1, it is also called attenuation.

Depending on the signal carrier type, we distinguish;

Power amplification	$V_P = \frac{P\,out}{P\,in}$
Voltage amplification	$V_u = \frac{P\,out}{P\,in}$
Current amplification	$V_i = \frac{P\,out}{P\,in}$

In practice, v>>1 is always being aimed at.

The amplifiers used in automation equipment must feature a considerable long−term stability. The amplification value set must not deviate to an extent beyond that permitted by the technological process to be influenced. The disturbances arising in the amplifier must be negligent compared to the signal values. This applies specifically to drift phenomena. A drift generally signifies the slow variation of a value by aging, temperature or supply voltage change.

Such disturbances can be minimized by negative feedback. But a negative feedback implies the danger of instability through self−exitation. It is necessary, therefore, to test the stability behaviour of the amplifiers. An easy possibility of doing so is to analyze the step response by means of an oscilloscope. For this purpose, a rectangular pulse featuring as steep edges as possible and a pulse frequency of some kilohertz is fed on the input, while an oscilloscope is connected to the output above the load resistor. Figure 45 shows some output pulse types and consequences to be derived therefrom.

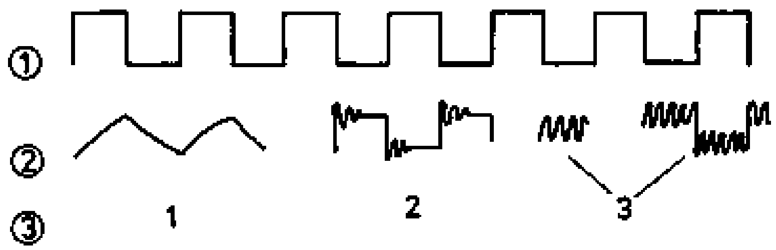


Figure 45 Analysis of the step response of an amplifier with respect to its stability

(1) input,
(2) output,
(3) conclusion
1 stable,
2 tendency towards instability,
3 instable

In addition to this practical method of testing the stability for self−exitation there are several other methods which, however, require higher theoretical or measuring−engineering efforts. Another method is presented in the Section "Operational amplifier" hereof.

Basic amplifier circuits

To build an amplifier, active components are required. Such components, almost all of which are transistors, control a supply energy so as to represent the respective signal. The higher signal energy on the amplifier's output is taken from this supply energy. Its source is the power supply unit which supplies its energy as direct current and direct voltage. Since the signal is time−dependent and part of the direct energy supplied by the power supply unit is converted into signal energy, i.e. alternating energy, there are direct and alternating quantities in an amplifier circuit, which are superimposed.

This results in pulsing D.C.

To make such pulsing D.C. possible, the active components are wired with additional passive components so that direct current is flowing through them even in unmodulated condition (a signal is not applied) and there are direct voltages between their electrodes. In the family of characteristics these D.C. quantities mark a point which is called bias point. The location of that bias point within the family of characteristics depends on the function of the respective amplifying stage. The amplifying stage is characterized as an active component with such additional components as are required for setting the bias point. Nearly all amplifiers have several stages. The active components used are transistors. The layout of the basic amplifier circuit depends on

– the basic circuit of the transistor
– the location of the bias point within the family of characteristics.

First let us look at the basic circuit of the transistor. Theoretically it is possible to use any of the three electrodes of a transistor as input or output for the signal. Considering that an amplification of v>>1 is required, in practice three basic circuits have been generally accepted. These three basic circuits are named after their common electrode for input and output.

Emitter circuit

Modulation with the signal energy is effected on the base; the amplified signal is picked up at the collector. The emitter is the common electrode for input and output. This circuit is the most important in practical use because the power amplification is the largest one and the input and output resistances of the transistor are about the same.

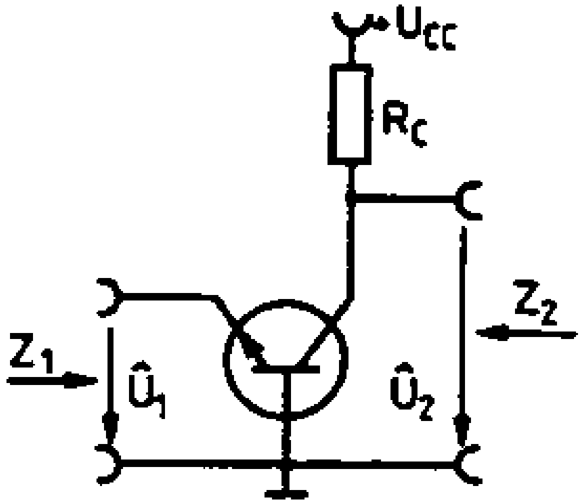


Figure 46 Emitter circuit

Collector circuit

Here, too, the signal is fed on the base, but the amplified signal is picked up at the emitter. The collector is the common electrode. This circuit is characterized by a high input and a low output resistance. It is, therefore, often used as impedance converter. The voltage amplification is $V_u \lessapprox 1$.

Since the potential at the emitter follows the potential at the base, this circuit is also called emitter follower.

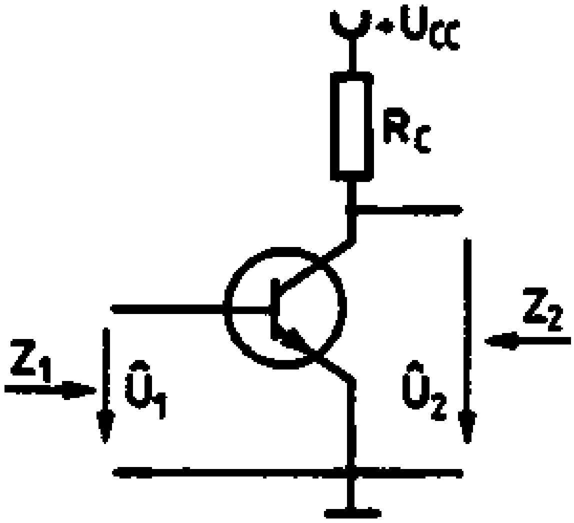


Figure 47 Collector circuit (emitter follower)

Basic circuit

In the case of this circuit, which is insignificant to automation engineering, the signal is fed at the emitter and picked up at the collector in amplified condition. The current amplification is v_i ? 1, the input resistance is low and the output resistance is equal to that of an emitter circuit.

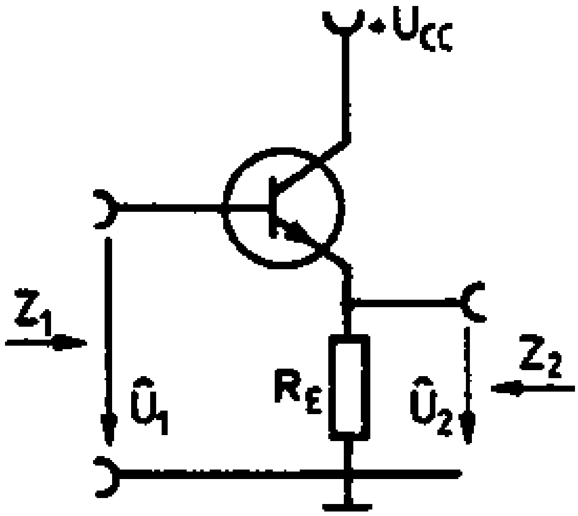


Figure 48 Basic circuit

The classification with field effect transistors is similar.

Source circuit

This circuit corresponds to the emitter circuit. The signal is fed at the gate and picked up at the drain.

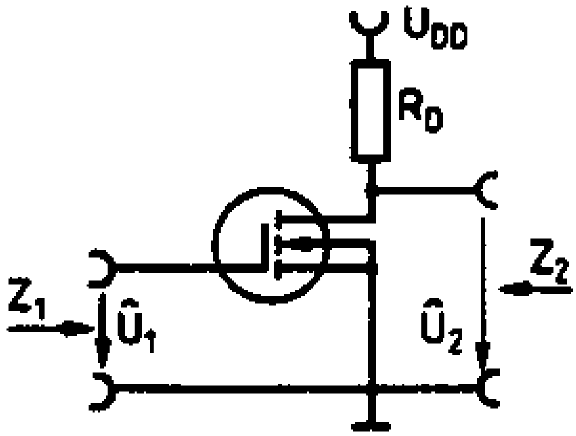


Figure 49 Source circuit

Table 4 Rated values of rectifier circuits

Circuit	D.C. output	Direct voltage	Ripple	Voltage load on diodes
	$I_{max.}$	$\frac{U_=}{U_1}$	%	$\frac{U_{RRM}}{U_=}$
Single–phase – single–pulse	$I_{F(AV)}$	0.45	121	3.14
Two–phase – two–pulse	$2I_{F(AV)}$	0.9	48	1.57
Two–phase – single–pulse	$2I_{F(AV)}$	0.9	48	3.14
Three–phase – single–pulse	$3I_{F(AV)}$	1.17	19	2.09
Three–phase – two–pulse	$3I_{F(AV)}3$	2.34	4	1.05

Table 5 Recommended operating values of basic transistor circuits

Emitter circuit	Collector circuit	Basic circuit
Z_1 ? 1...10 k?	Z_1 ? 100...1000 k?	Z_1 ? 10...100 k?
Z_2 ? 10...100 k?	Z_2 ? 10...100 k?	Z_2 ? 100...1000 k?
v_u ? -10^2	v_u ? 0.98 ? 1	v_u ? 10^2
v_1 ? 10^2	v_1 ? -10^2	v_1 ? –0.98 ? –1
v_p ? 10^4	v_p ? 10^2	v_p ? 10^2
?u2 u1 = –180°	?u2 u1 = 180°	?u2 u1 = 0°

Source circuit	Drain circuit	Gate circuit
Z_1 ? ?	Z_1 ? ?	Z_1 ? 500?
$Z_2 = R_D$	$Z_2 = R_S$	Z_2 ? R_D
V_u ? -10^2	V_u ? 0.9	V_u ? 10
V_1 ? ?	V_1 ? –?	V_u ? –1
Minus sign ≙ 180 deg. phase rotation (output – input)		

Drain circuit

Like the collector circuit, which corresponds to this circuit, the drain circuit is also called source follower. Because of the high input resistance of a MOSFET, which for D–C. voltages is about Z_1 ? $10^{12}...10^{14}$?, it is possible to achieve extremely high input resistances of the entire circuit.

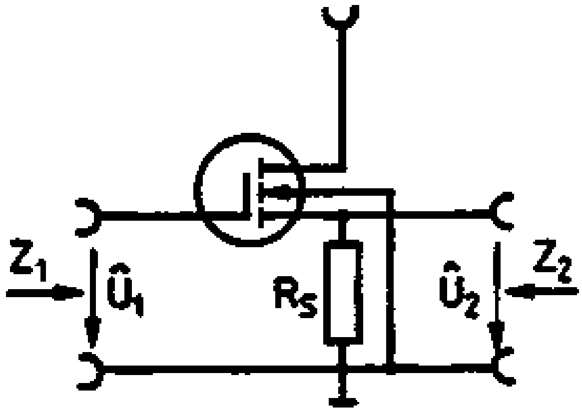


Figure 50 Drain circuit (source follower)

Gate circuit

Corresponding to the basic circuit, this circuit, too, is rather insignificant to automation engineering.

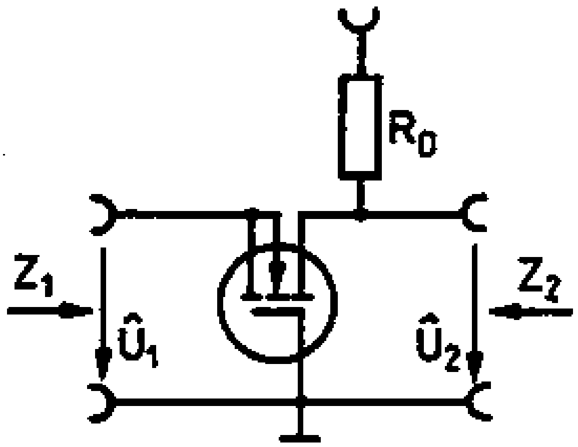


Figure 51 Gate circuit

Table no. 5 contains some reference values for the operating values of the basic circuits.

The location of the bias point, the mode of operation, determines the modulation possibility of the amplifying stage. Some of the modes possible are shown in Figure 52.

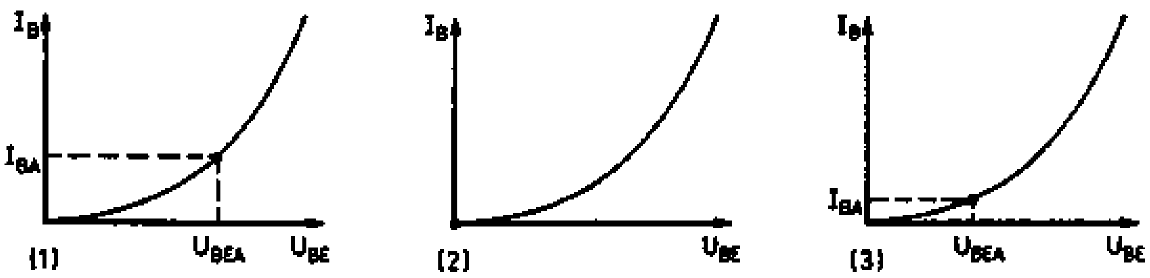


Figure 52 Modes of operation of transistors in amplifier stages

(1) A–mode,
(2) B–mode,
(3) AB–mode

For automation engineering, the A– and the B–mode are of practical importance. The A–mode permits to transmit positive and negative variations of the signal. In this mode preamplifiers are utilized. The B–mode permits the transmission of but one variation (positive or negative) of the signal. The push−pull interconnection of two transistors, one of which is to transmit the positive and the other one the negative variations, permits a universal modulation in the B−mode, too. But in automation engineering this is not always necessary. Modulation in but one direction is sufficient, e.g. for transmitting a standard signal the polarity of which remains unchanged.

Static calculation of an amplifying stage

When calculating an amplification the bias point temperature is to be set and stabilized first. Such calculations are also called static calculations. Due to the transistor parameter being temperature−dependent, the temperature is to be stabilized, In the case of bipolar transistors this refers particularly to the temperature dependence of the base−emitter−voltage. As a general rule, for Si transistors a temperature coefficient of TK_{uBE} ? −2 mV. K^{-1} is to be applied. Consequently, in order to keep the collector amperage constant, the base−emitter−voltage is to be reduced by ? 2 mV per degree of temperature rise. The tolerance of the direct current amplification of $B = h_{21E}$ with bipolar transistors or of the mutual conductance of y_{21} with field effect transistors is to be considered in the calculations, They, too, have an influence on the location of the bias point.

Selection of the bias point within the family of characteristics

In addition to the selected mode of operation (A− or B−mode), the following factors are to be considered:

− The power dissipation arising without modulation (standby power dissipation).

This power dissipation can be kept small by a low collector amperage I_{CA} and a low collector voltage U_{CEA}. Figure 53 shows e.g. that the power dissipation in point A. is larger than that in point A_2.

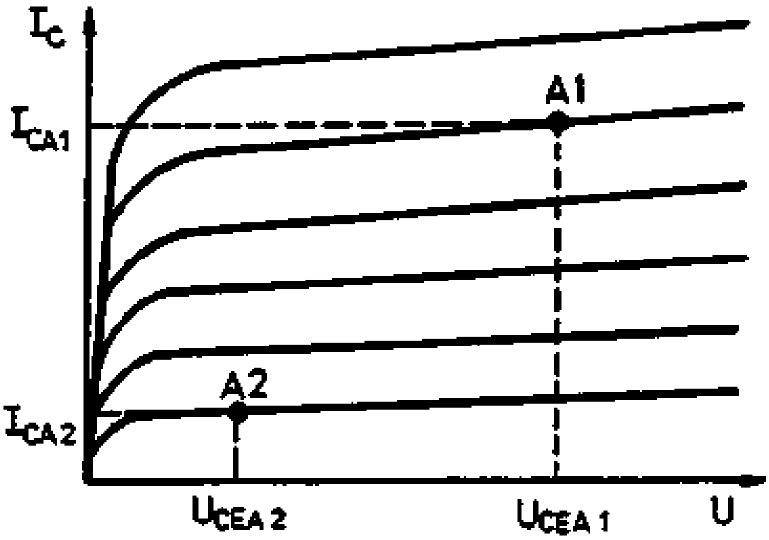
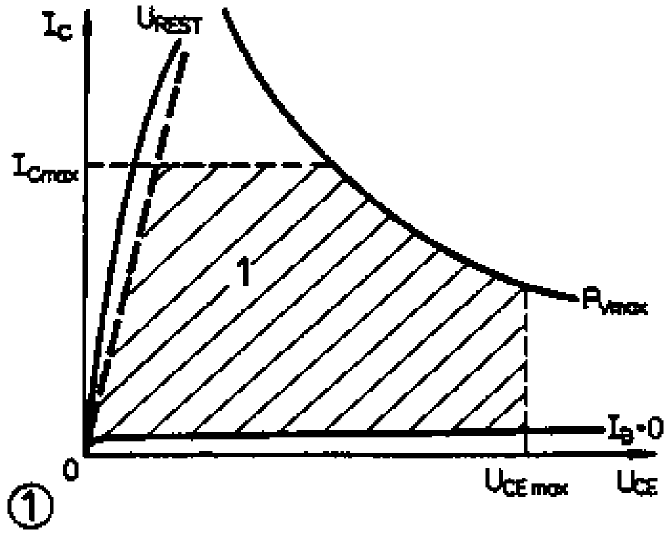


Figure 53 Standby power dissipation in dependence on the bias point

− The alternating amplitude arising.
Large amplitudes require high D.C. values in the bias point< To permit positive and negative variations to be constantly transmitted, the bias point must be symmetrical to the modulation limits which are represented in Figure 54.



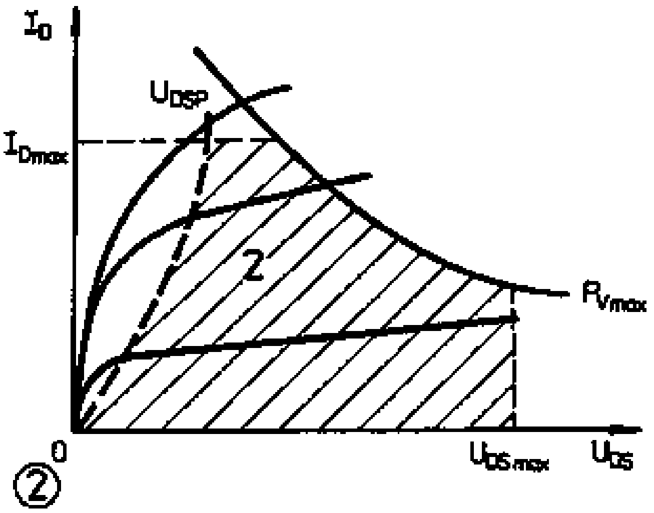


Figure 54 Working range (modulation limits)

(1) for bipolar transistors,
(2) for unipolar transistors
1 working range,
2 working range as amplifier

Other criteria, such as minor distortions, are unimportant to automation engineering. Within the hatched fields any location can be selected for the bias point.

Upon selection of the bias point, which can be transferred into the respective quadrants of the complete family of characteristics (Figure 55), the required values are read from the family of characteristics.

U_{CEA}	collector voltage in the bias point
I_{CA}	collector amperage in the bias point
U_{BEA}	base voltage in the bias point
I_{BA}	base amperage in the bias point

All voltages refer to the emitter.

U_{DSA}	drain voltage in the bias point
I_{DA}	drain amperage in the bias point
U_{GSA}	gate voltage in the bias point

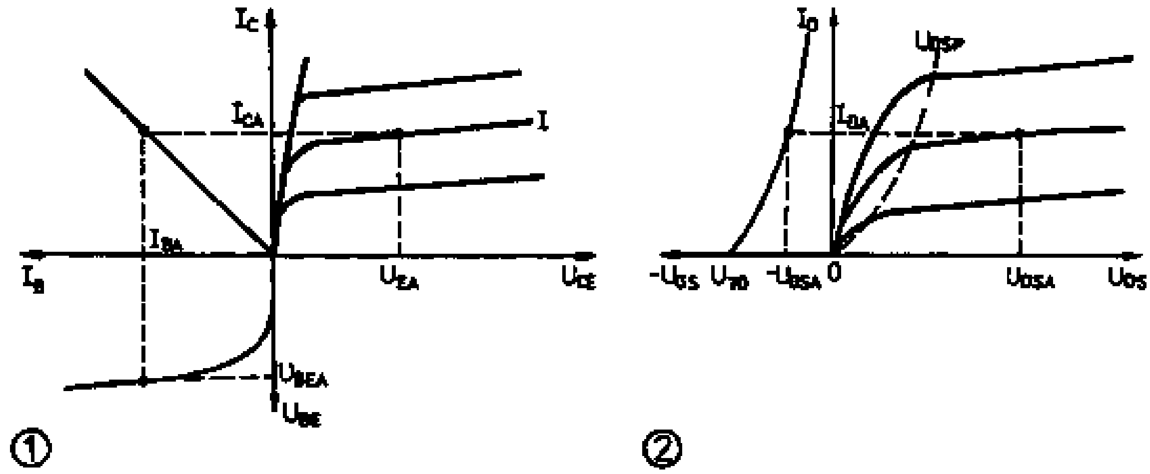


Figure 55 Transfer of the bias point to other families of characteristics

(1) for bipolar transistors,
(2) for field effect transistors (n−channel depletion type)

All voltages refer to the source. The input amperage I_{GA} is zero. A suitable layout of the circuit is to ensure that these selected values can be achieved.

<u>Bias point setting by means of a base dropping resistor</u>

The amperage of the required base current I_{BA} is determined by R1 which keeps it also constant. The base voltage U_{BEA} arises automatically.

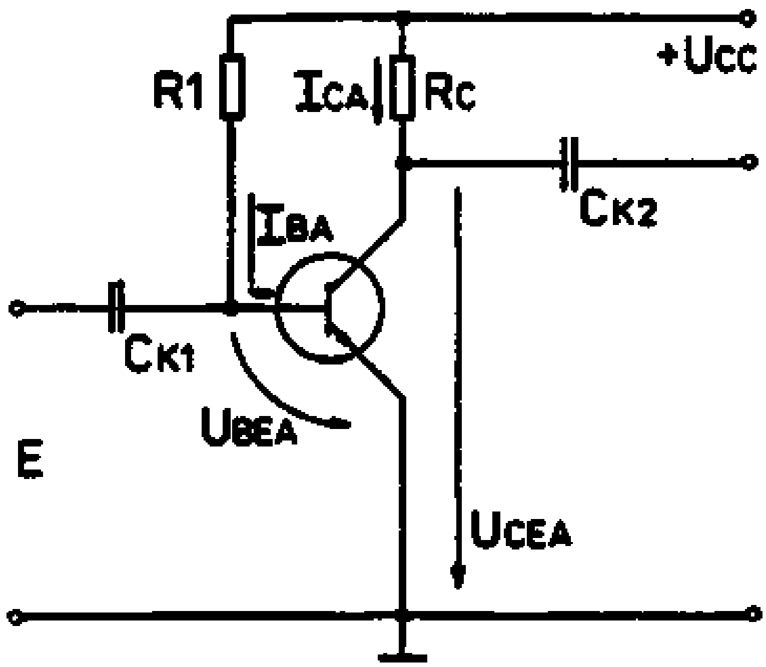


Figure 56 Bias point setting by means of a base dropping resistor

The resistance are calculated by means of the following equations:

$$R_1 = \frac{U_{CC} - U_{BEA}}{I_{BA}}$$

$$R_C = \frac{U_{CC} - U_{CEA}}{I_{CA}}$$

Due to $I_{CA} = B\ I_{BA} = h_{21E}IB_A$ and the constant base amperage (power supply), the bias point in this circuit is not stabilized in the event of variations in the power amplification B. This type of bias point setting is therefore employed with simple amplifiers only.

The coupling capacitors C_{K1} and C_{K2} separate the stage in terms of D.C. voltage from preceding or following circuit parts.

<u>Bias point setting and stabilization by means of direct current negative feedback</u>

This circuit is frequently employed in preamplifiers and can be called a standard circuit. In this circuit the bias point is set and, at the same time, stabilized via R1, R2 and R_E. The stabilization is effective against temperature changes and power amplification tolerances and is the better, the higher U_{RE}. U_{RE} is to be selected in the range from 0.5 to 2 volts. Since the base voltage divider R1/R2 is to stabilize the base potential, the transverse current of I_q ? (5...10) I_{BA} is selected.

If so, any variation of the collector voltage brings about a variation of the partial voltage through R_E which, in turn, changes U_{BE} so as to nullify the collector amperage variation. The negative feedback principle, which is effective here, is explained in more detail later on.

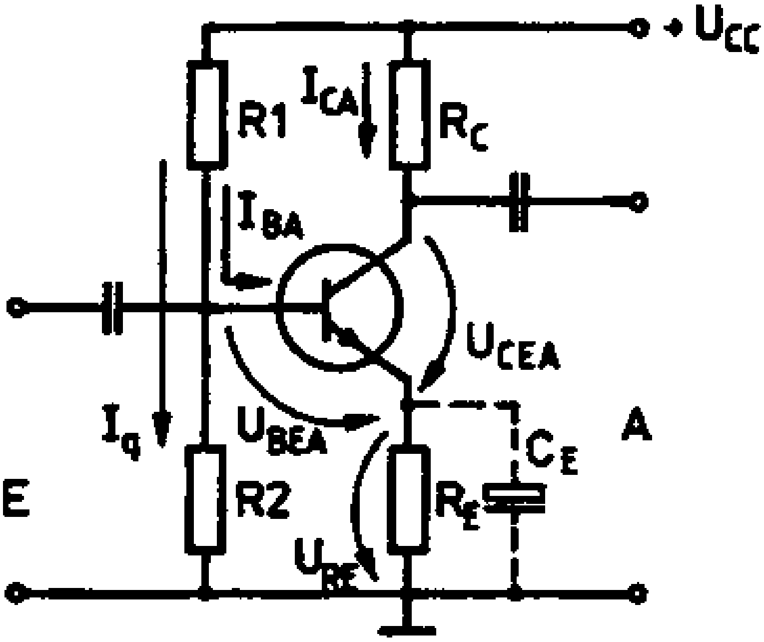


Figure 57 Bias point stabilization by means of direct current negative feedback

As to the calculation, the following equations are to be used:

I_q ? (5...10) I_{BA}

U_{RE} ? 0.5...2 V

$$R_E = \frac{U_{RE}}{I_{CA} + I_{BA}} \approx \frac{U_{RE}}{I_{CA}}$$

$$R_C = \frac{U_{CC} - U_{CEA} - U_{RE}}{I_{CA}}$$

$$R_1 = \frac{U_{CC} - U_{BEA} - U_{RE}}{I_Q + I_{BA}}$$

$$R_2 = \frac{U_{RE} + U_{BEA}}{I_Q}$$

The equations are derived from the mesh principle. This shall be demonstrated by means of an example.

As to the mesh cycle shown in Figure 58, the formula is:

$R_1 (I_q + I_{BA}) + U_{BEA} + U_{RE} - U_{CC} = 0.$

Re−formularizing this, you can easily derive R_1.

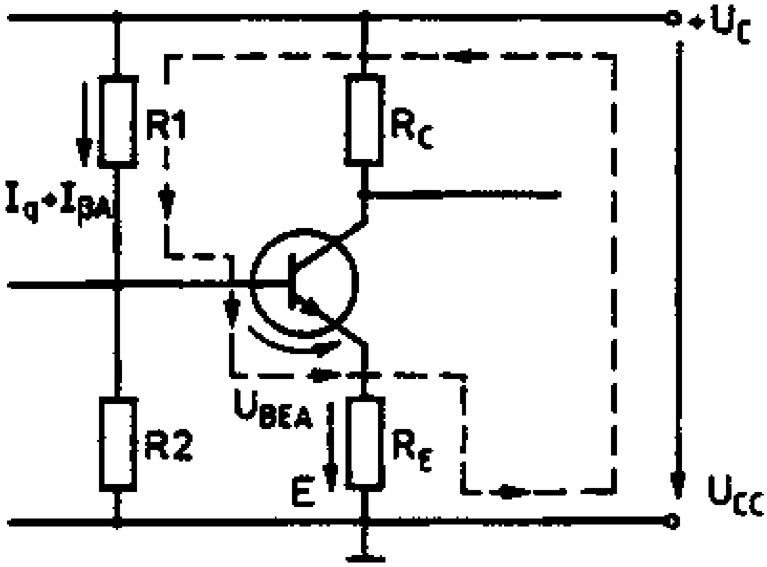


Figure 58 Application of the mesh principle for the calculation of R1

In addition to the D.C. negative feedback, which is desired and causes the bias point to stabilize, an A.C. negative feedback, which is undesired, occurs that is eliminated by bridging the emitter resistance R_E by a high capacitance C_E.

This capacitance is represented in Figure 57 by dashed lines.

<u>Stabilization using the half−supply−voltage method</u>

An amplifying stage is temperature−resistant in the event of the amount of heat dissipated being larger than or equal to that supplied.

Q dissipated ? Q supplied

For a transistor with a collector resistance R_C the dissipation can be determined from

$$P_V = U_{CEA} \cdot I_{CA} = U_{CEA} \frac{U_{CC} - U_{CEA}}{R_C} = \frac{U_{CC} \cdot U_{CEA}}{R_C} \cdot \frac{U_{CEA}^2}{R_C}.$$

The maximum dissipation occurs in the event of

$$U_{CEA} = \frac{U_{CC}}{2}.$$

In such a case, a re−location of the bias point by temperature influences always results in a smaller dissipation with the transistor.

An amplifiying stage is temperature−resistant in the event of $U_{CEA} = \frac{U_{CC}}{2}.$

A stabilization by this method is possible only with ohmic collector resistances. It is ineffective in the event of the bias point being changed for other reasons. Bearing this in mind, this method is applicable to a limited extent, only.

<u>Bias point setting and stabilization through non−linear resistors</u>

These circuits, too, can compensate temperature−dependent variations only. Their basic concept is to adapt the temperature coefficient of the transistor basic wiring to that of the − transistor. Consequently, the base−emitter−voltage is to be reduced by about 2 mV per degree of temperature rise, which, in turn, requires a good thermal contact between the non−linear resistor and the transistor.

Figure 59 (1) shows a circuit featuring an NTC resistor. The resistances R_r and R_p can be roughly calculated only; the tolerance of the NTC resistor's temperature dependence is ± 20%. Due to these shortcomings, the resistor R2 in the base voltage divider has been replaced by a diode that is operated in the direction of flux. In the event of this diode consisting of the same semiconductor material as the transistor and having also the same temperature, it features the same flow voltage variation as the transistor.

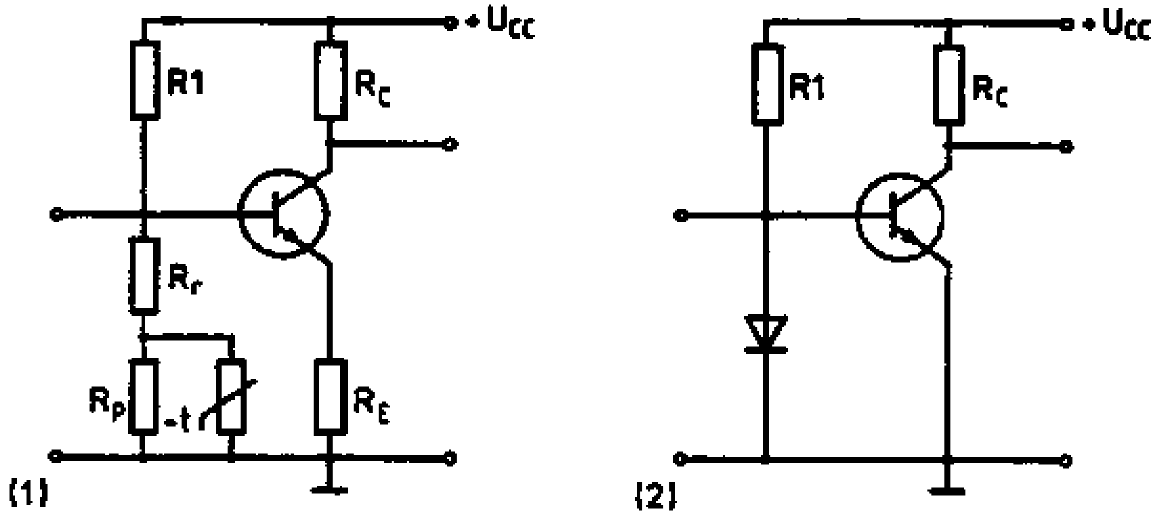


Figure 59 Bias point stabilization by means of a non−linear resistor

(1) NTC resistor,
(2) diode

The circuits shown in Figure 60 can be termed standard circuits of a preamplifying stage. Additional features on this drawing are the signal generator with its source resistor R_Q and loading of the stage by a load resistor R_A.

Once more, the circuits illustrate the function of the coupling capacitors C_{K1} and C_{K2} to separate the D.C. voltage from the stage.

When calculating the resistances for the standard circuit with a MOSFET (Figure 60 (2)), the type of conductivity (p−or n−channel) and the design (either enhancement or depletion type) are to be considered.

For a depletion type − in order to pinch off the channel − the gate voltage must have the same polarity as the charge carriers in the channel. In the case of an n−channel this means a negative voltage. For the enhancement type the polarity of the gate potential must be contrary to that of the channel charge carriers if a channel is to be developed.

Figure 60 (2) represents a universal circuit which is applicable to both (enhancement and depletion) types. Selecting suitable Values, the voltage divider R1/R2 and the resistor R_S permit a positive or negative potential of the gate against the source.

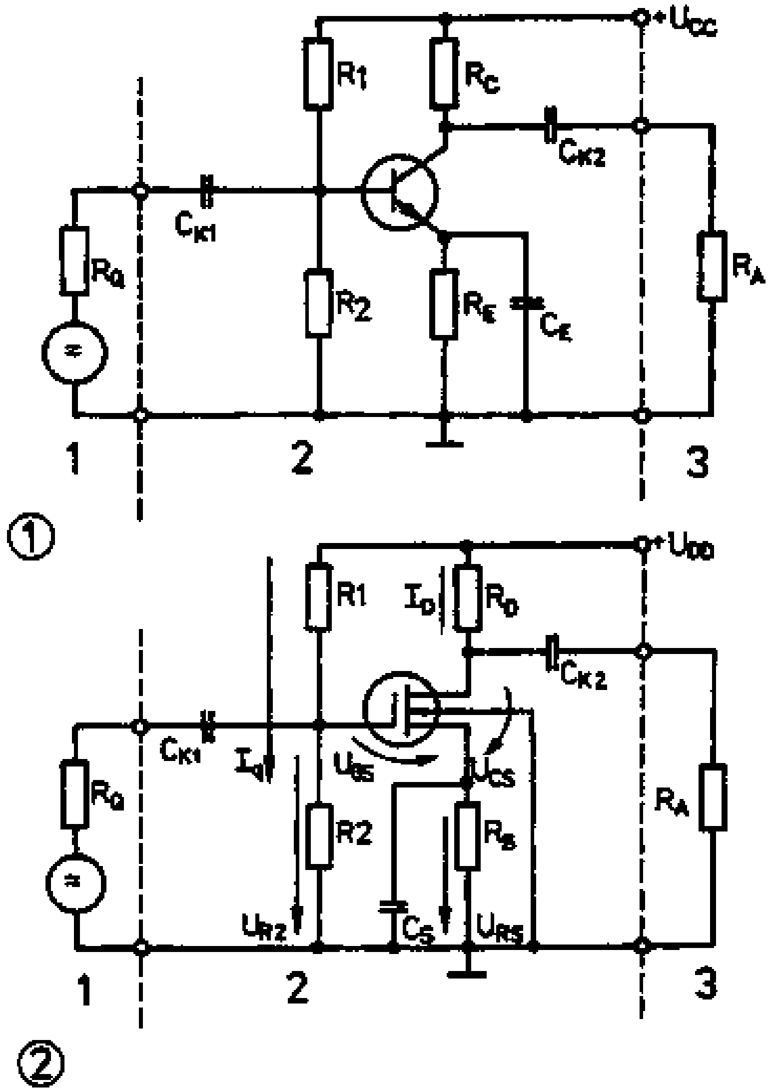


Figure 60 Amplifier stage in a standard circuit with generator and termination resistance

(1) with bipolar transistor
(2) with n−channel MOSFET (depletion type)
1 source (generator)
2 amplifier stage
3 termination (load)

Heeding the signs of the partial voltage and currents the following equations are to be employed:

$$R_D = \frac{U_{DD} - U_{DSA} - U_{RS}}{I_{DA}}$$

$$R_S = \frac{U_{R2} - U_{GS}}{I_{DA}}$$

$$R_2 = \frac{U_{R2}}{I_q}$$

$$R_1 = \frac{U_{DD} - U_{R2}}{I_q}$$

The voltage divider transverse current I_q is freely selectable; the reference value is I_q ? 0.1 ...µA.

From the A.C. voltage point of view, the transistor is not effective alone, any more, but in connection with the circuit which is necessary to set the bias point. Following the static consideration, therefore, a dynamic consideration is to be made in order to study the influence of the additional components on the A.C. behaviour of the transistor.

<u>Dynamic calculation of an amplifying stage</u>

Let us first explain by means of a diagram how an amplification can be achieved with the given basic circuit. Here, too, the family of characteristics is utilized. It is indicated by the manufacturers or measured and, if stated by the manufacturers, applies to a medium−range transistor. The effect of the transistor wiring necessary for setting the bias point must be entered into the existing family of characteristics. The resistors acting in the D.C. collector circuit are represented in Figure 61. With the selected mesh cycle this results in:

$U_{RC} + U_{CE} + U_{RE} - U_{CC} = 0$

$I_C R_C + U_{CE} + I_E R_E - U_{CC} = 0$

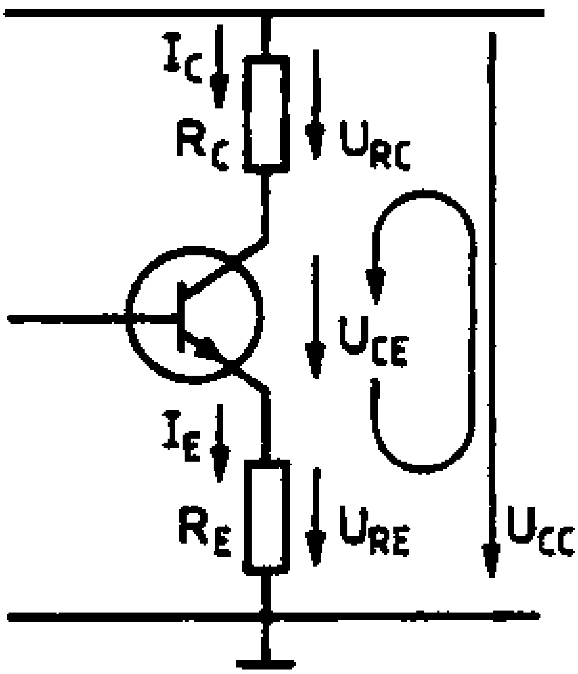


Figure 61 Partial voltages in a collector circuit

It is possible to approximately equate the collector amperage with the emitter amperage because the power of the base current is considerably lower.

$I_E = I_C + I_B$? I_C

This makes

$$U_{CC} - U_{CE} - I_C (R_C + R_E) = 0$$
$$U_{CE} = U_{CC} - I_C (R_C + R_E)$$

and it serves as reference for entering the resistance lines into the family of characteristics. From the complete family of characteristics that part can be used for such purpose only in which the parameters I_C and U_{CE} are interconnected. This part is the output family of characteristics of the transistor. The graphic representation leads to a line because the parameters are linear ones, only. A line is clearly determined when two points of it are known. In this connection, it is advisable to use the intersections with the coordinate axes.

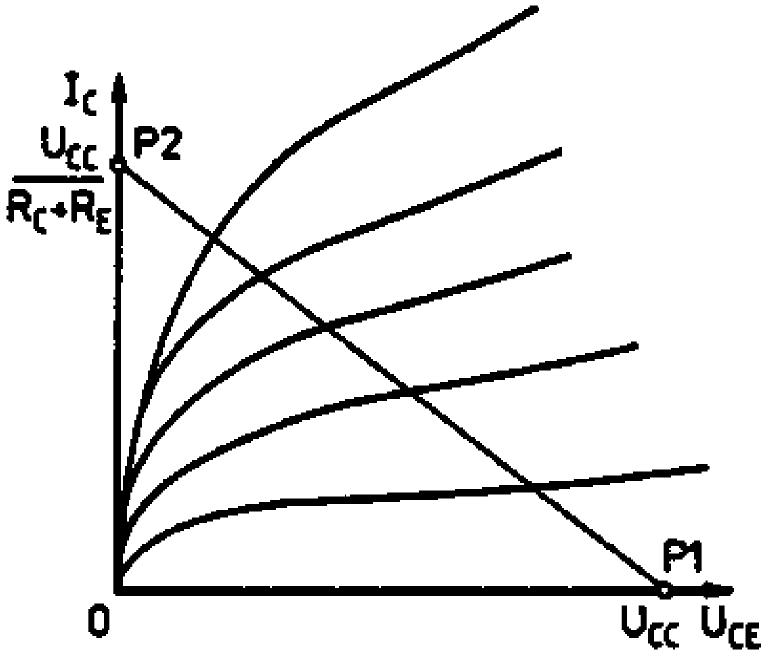


Figure 62 Resistance line in the family of output characteristics

Let point P1 be

$I_C = 0$.

This makes

$U_{CE} – U_{CC}$.

Similar to that, let point P2 be

$U_{CE} = 0$

$$I_C = \frac{U_{CC}}{R_C + R_E}.$$

Supposed that $R_C >> R_E$ we can simplify I_C to

$$I_C = \frac{U_{CC}}{R_C}.$$

Connecting the points P1 and P2 we receive the resistance line $R_C + R_E$ or R_C,respectively.

When selecting a bias point the electrical conditions of the transistors are to be complied with. This means that the bias point must be nowhere but on the intersections of the resistance line with the transistor characteristics, i.e. on the resistor line itself, since the electrical conditions of the transistor are expressed by its characteristic.

The resistance line $R_C + R_E$ shown in Figure 62 was determined for direct current only and, therefore, exclusively applies to D.C. values.

In the event of modulation with a signal, which in almost every case is an A.C. value, the conditions are different. To determine these conditions, an equivalent A.C. circuit is drawn for the basic circuit. In this connection, attention is to be paid to the fact that the power supply unit must always be designed with a negligibly low internal A.C. resistance. This is achieved, e.g., by the filter capacitor the high capacitance of which makes a low reactance possible. The positive and negative poles of the alternating current of the power supply unit, therefore, are on the same potential (almost exclusively an earth potential). These conditions are outlined in Figure 63 (1) and considered in Figures 63 (2), In Figure 63 (3) the medium frequencies, at which the capacitances of the coupling and the emitter capacitors become so low as to almost impliying a short−circuit, are represented in a simplified version. Now the transistor is loaded with the parallel circuit of R_C and R_A at the collector. For this the term <u>load resistance</u> R_L is introduced.

$$R_L = R_C // R_A = \frac{R_C R_A}{R_C + R_A}$$

When the transistor is modulated, the load resistance R_L is acting.

This load resistance can also be drawn into the family of characteristics as a line. Here, too, two points are sufficient. One of these points is the bias point, for the values marked by it apply if there is no modulation.

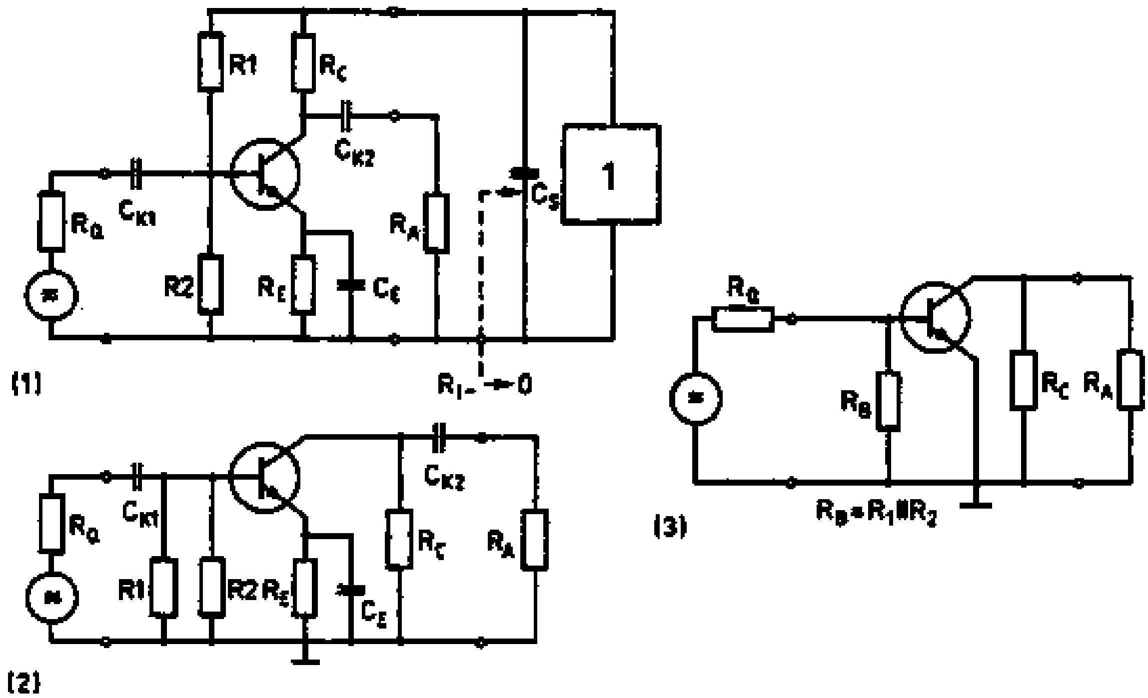


Figure 63 Transition from the circuit diagram to the equivalent circuit layout

(1) circuit diagram,
(2) A.C. equivalent circuit layout,
(3) simplified version for medium frequencies
1 power supply unit

The other point can be determined by taking also the modulation into account (by ? values).

In the event of a field effect transistor instead of a bipolar transistor being applied, the same procedure is to be followed. Since there is no input current, the family of output characteristics is sufficient for a MOSFET. Figure 64 shows the ratios for an n−channel depeltion type in a source circuit. The illustration also shows the modulation in the family of transfer characteristics. It is advisable to select the bias point so as to permit a symmetrical modulation along the R_L line. The graphic method of determining the amplification is very descriptive and, therefore, was explained herein at length. In practice," the amplification is more often determined by calculation, using the quadripole parameters of the transistor or other specific quantities. To aim at exact results is of little use, here, because

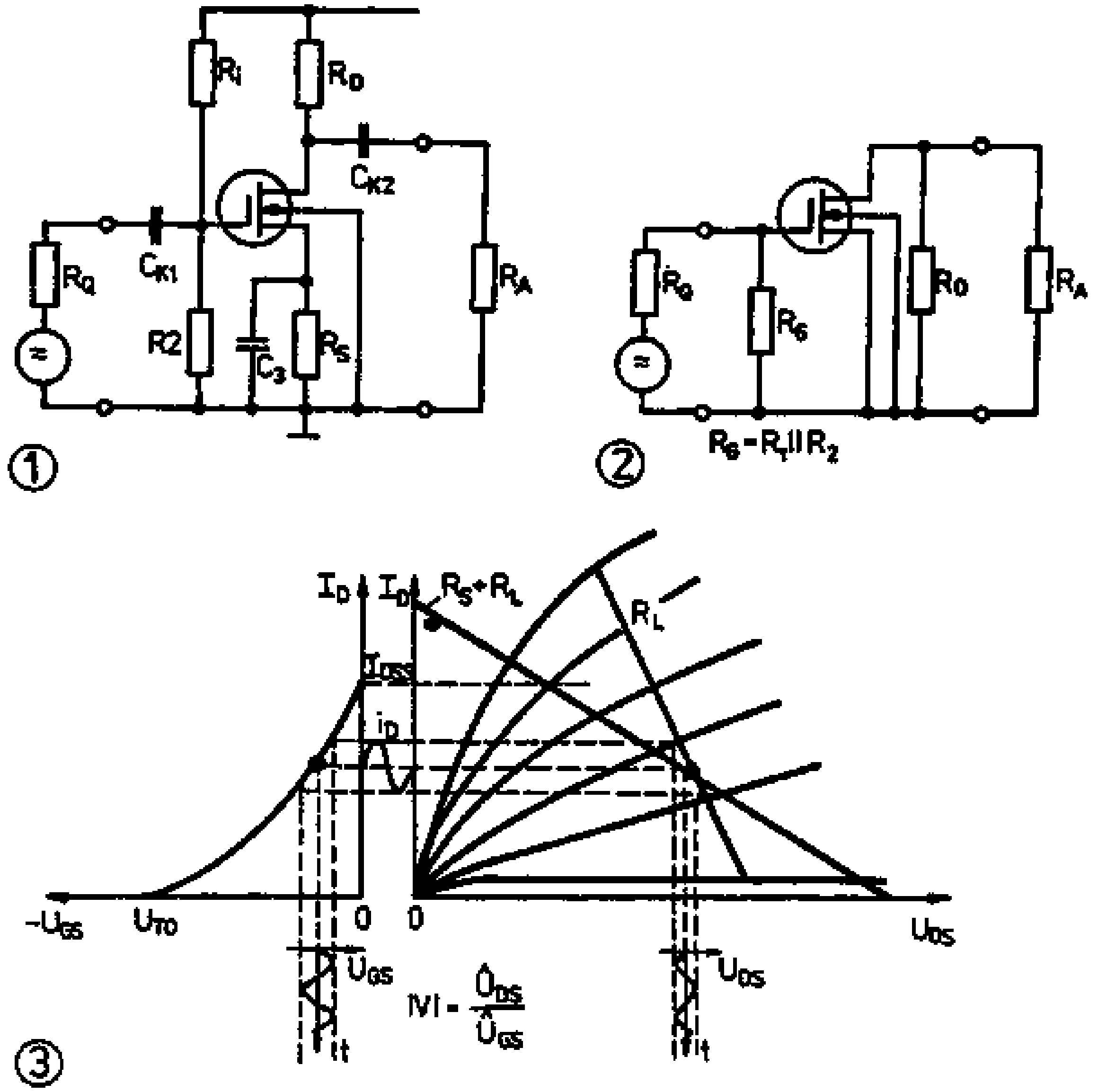


Figure 64 Modulation in the family of characteristics of an n–channel MOSFET (depletion type)

(1) basic circuit,
(2) A.C. equivalent circuit layout for medium frequencies,
(3) graphic representation in the families of characteristics

– the transistor data indicated by the manufacturers are mean values only, which may vary by up to +/– 40% (current amplification) from transistor to transistor;

– the additional components to be used are subject to tolerances, Usually they are selected from the E 12 range (tolerances of +/– 10 %).

In many cases a rough estimation will do. Moreover, modern semiconductor components can be considered in a simplified way in respect of frequencies of up to some 10 kHz. Such consideration is permitted in automation engineering.

If the quadripole parameters are used for calculation, therefore the h–parameters are employed only. The voltage reaction h_{12e} and the output admittance h_{22e} can usually be neglected. However a calculation is admitted only if there is a small–signal modulation.

The basic circuit is changed into a quadripole basic circuit as I shown in Figure 65. The resistances at the base end are concentrated to form the source resistance R_G, while those at the collector end are concentrated to form the load resistance already known. The transistor is represented as quadripole with h–parameter. The calculations are always made for medium frequencies.

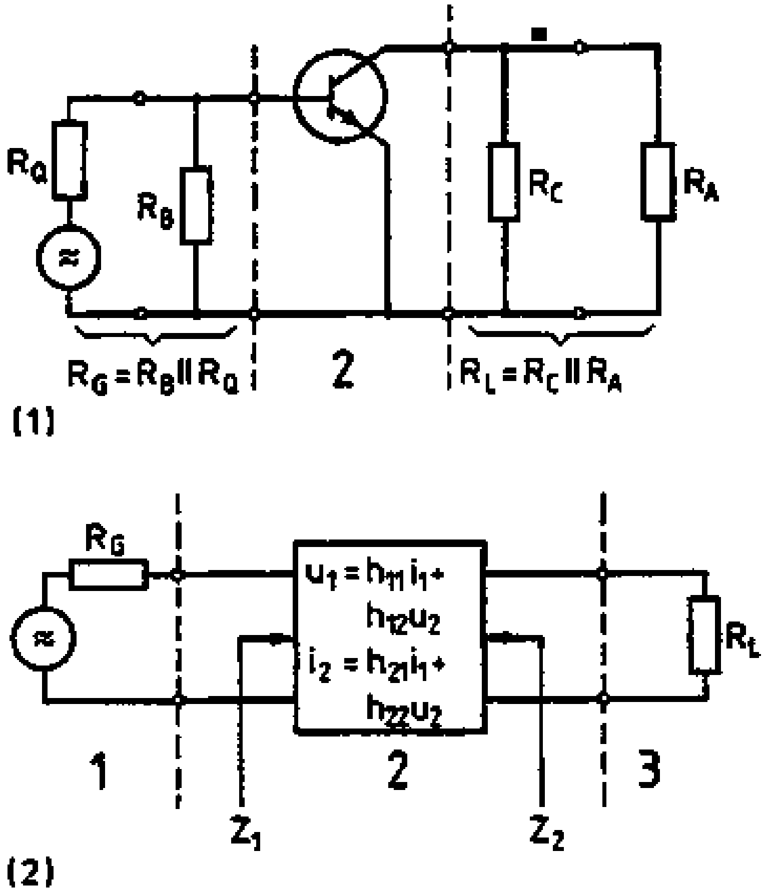


Figure 65 Transition from the simplified A.C. equivalent circuit layout to the quadripole basic circuit

(1) simplified A.C. equivalent circuit layout,
(2) quadripole basic circuit
1 source,
2 transistor,
3 load

As far as high frequencies are concerned, the inevitable wiring capacitances become apparent which form a low passfilter with the resistances or short the signal path.

In addition to that, the short–circuit amplification h_{21} is frequency–dependent. It is the smaller, the higher the frequency.

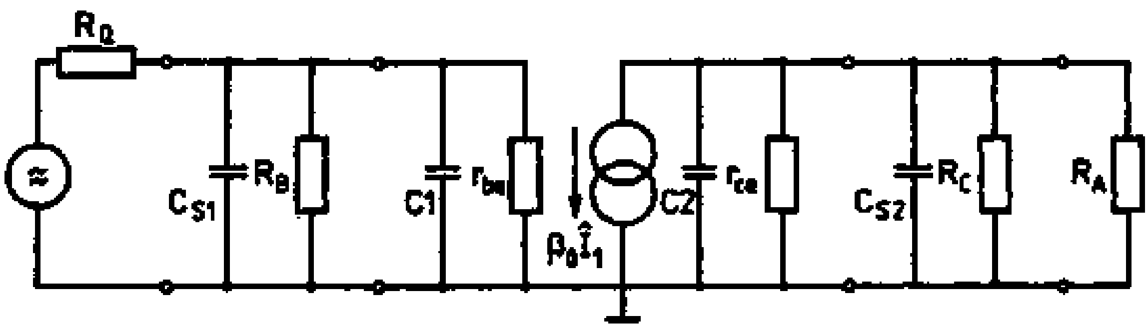


Figure 66 Equivalent circuit layout of an amplifier stage with high frequencies

C_{S1}, C_{S2} switching capacitances, C_1 input capacitance of the transistor, C_2 output capacitance of the transistor

In principle, the dependence of the amplification on the frequency, the amplitude characteristic is as shown in Figure 67.

Generally, the frequency where the current or voltage amplification is dropped to $\frac{1}{\sqrt{2}}$ times its value for medium frequencies, is called cut−off frequency f_q.

The low−frequency cut−off is called f_u while the high−frequency cut−off is called f_o.

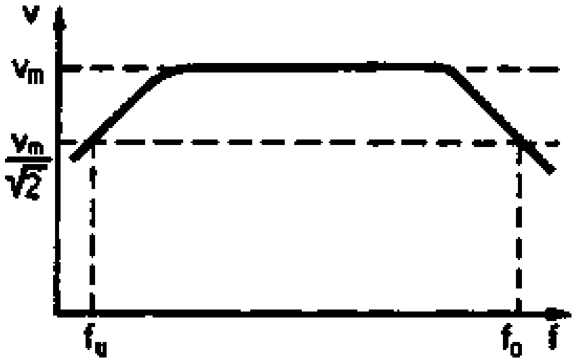


Figure 67 Amplitude characteristic of an amplifier

It is not necessary to calculate the high−frequency cut−off for frequencies of up to some hundreds of kilohertz, for it is always attained by silicon transistors.

For automation engineering purposes the frequency range under consideration will do. For this reason, further data regarding the high−frequency cut−off will not be mentioned in this book.

$$f = f_g, \text{ if } \frac{v(f)}{v_m} = \frac{1}{\sqrt{2}} = a$$

v(f) stands for amplification with frequency f

v_m stands for amplification in the medium frequency range

A <u>dropping−off spot</u> is a spot of the amplifying stage where the amplification is influenced depending on the frequency, i.e. on the coupling capacitors and on the emitter capacitor at low frequencies.

If several dropping−off spots are to be considered in the calculation, they are usually expressed as logarithmic quantity, as <u>level</u>. The level is indicated in dB (decibel).

$$p = 20 \lg \frac{v(f_g)}{v_m} = 20 \lg \frac{1}{\sqrt{2}} = -3\text{db}$$

The amplitude (or amplification) drop to $a = 1/\sqrt{2}$ corresponds to a level of p = – 3dB. This is the total drop admitted with the cut−off frequencies. Consequently the drop with each dropping−off spot must be less than −3 dB. Using the level, the individual drop−offs are added up. They can be easily determined so as to come up to a sum of p = −3 dB.

Using the real values, the individual drop−offs have to be selected so as to come up to a result of $a = 1/\sqrt{2}$. For each dropping−off spot the drop−off in dB is to be selected so as to come up to the admitted total drop−off.

The equations required for calculating an amplifying stage according to Figure 68 are as follows:

$$C_{K1} = \frac{1}{2\pi f_u \left(R_Q + R_B // r_{be}\right)} \cdot K$$

$$C_{K2} = \frac{1}{2\pi f_u \left(R_A + R_C // \frac{1}{h_{22e}}\right)} \cdot K$$

$$K = \frac{a_K}{\sqrt{1 - a_K^2}}$$

$$a_K = \frac{P_K}{10^{20}}$$

P_K stands for the drop−off in dB selected for the respective spot.

The emitter capacitor is calculated using the following equation:

$$C_E = \frac{1}{m 2\pi f_u R_E} \quad \sqrt{\frac{a_E^2 - m^2}{1 - a_E^2}}$$

$$m = \frac{h_{11e}}{h_{11e} + h_{21e} R_E} \approx \frac{r_d}{r_d + R_E}$$

$$a_E = \frac{P_E}{10^{20}}$$

P_E stands for the drop−off in dB admitted for the emitter combination.

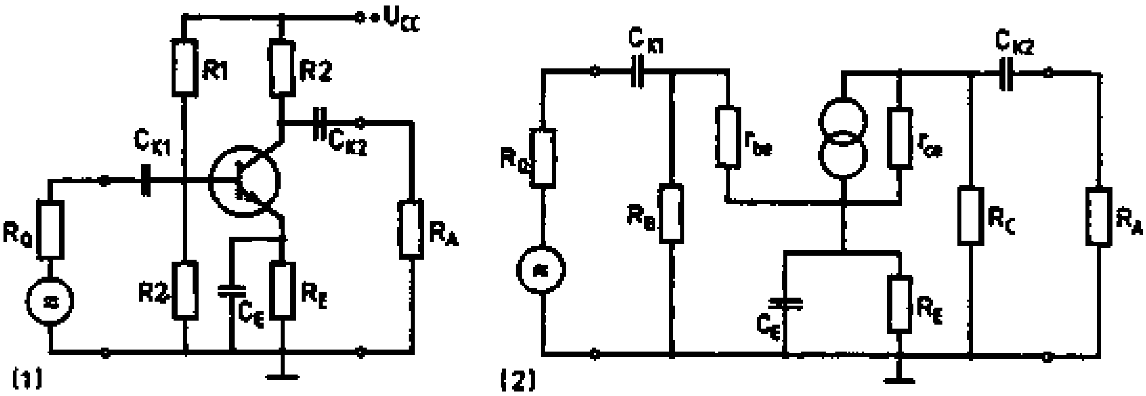


Figure 68 Calculation of the coupling and emitter capacitors

(1) circuit layout of an amplifier stage,
(2) A.C. equivalent circuit layout for low frequencies

1.4.3. Back−coupling

The term "back−coupling" signifies the interconnection of an amplifier's output with its input.

An intended back−coupling is also called "feedback" , and thus differs from an unintended back−coupling, which is called "reaction". A back − coupling is possible in such a way that the power fed back to the input is in phase with or opposite in phase to the input power.

The basic structure in Figure 69 results in

$$\underline{K}_P = \frac{\underline{x}_a}{\underline{x}_e} = \frac{\underline{K}_{P1}}{1 \pm \underline{K}_{P1} \underline{K}_{P2}},$$

which in amplification technology is expressed this way:

$$\underline{v}' = \frac{\underline{\hat{U}}_2}{\underline{\hat{U}}_1} = \frac{\underline{v}}{1 \pm \underline{v}\,\underline{k}}$$

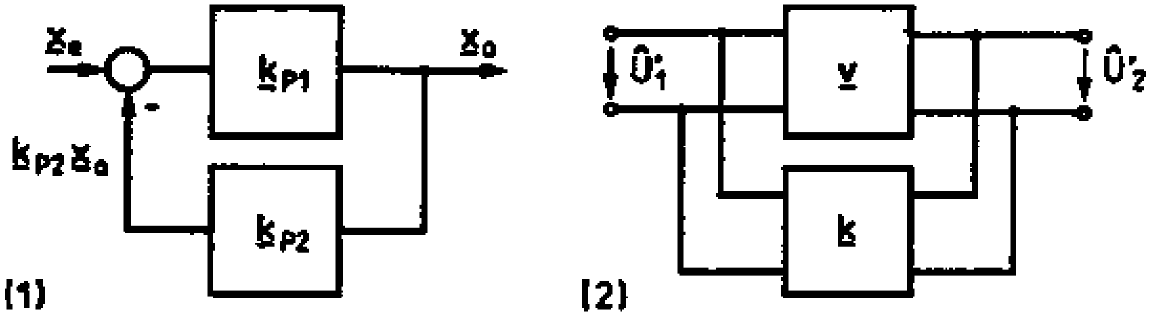


Figure 69 General structure of back−coupling

(1) representation usual in automation engineering
(2) representation usual in electronics

In this connection, the plus sign applies to the opposite−in−phase feedback, which is then called negative feedback, while the minus sign stands for the in−phase feedback, which is called positive feedback.

$$\text{negative feedback} \quad \underline{v}' = \frac{\underline{v}}{1 + \underline{v}\,\underline{k}}$$

$$\text{positive feedback} \quad \underline{v}' = \frac{\underline{v}}{1 - \underline{v}\,\underline{k}}$$

The value fed back is marked by a stroke. Being preferred in feedback technology, only the 0 and 180° phase positions are referred to herein, with any other phase shift being possible, too.

Of special importance to amplifiers is the negative feedback, for it has the following advantages:

− The circuit becomes resistant against aging, supply voltage fluctuations, drastic scattering of the component parameters and temperature variations.

− The frequency response is extended.

− The signal shape distortions are reduced.

− It is possible to change the input and output resistances of the transistor.

A negative feedback has the disadvantage, however, of reducing the gain in an amplifier stage. But taking into account the many advantages, amplifiers are always fed back negatively, in practice.

The product $\underline{v}$ $\underline{k}$ is termed <u>loop gain</u> $\underline{v}_s$

$\underline{v}\ \underline{k} = \underline{v}_{s'}$

the expression "1 + $\underline{v}$ $\underline{k}$" is termed <u>negative feedback ratio</u> g

$1 + \underline{v}\ \underline{k} = g.$

The negative feedback gains in importance particularly if the gain v becomes extremely high. Then the following applies:

lim v' = 1/k

v ? ?

The gain v' does not depend on v any more. The feedback network can be built using stable passive components (resistors), the behaviour of which determines the gain v'. This is the way to design highly stable measuring amplifiers. The power fed back can be derived either from the output voltage or from the output current. Consequently, we speak of either negative <u>voltage</u> feedback or negative <u>current</u> feedback. These two types act differently on the amplifier.

<u>Negative current feedback</u>

A negative current feedback is characterized by an emitter resistance which is not bridged by a capacitor. When only part of the emitter resistance is bridged capacitively, a modified circuit is produced according to Figure 70 (2). Its advantage is that the negative direct–current feedback for temperature stabilization of the bias point ($R_E = R_{EI} + R_{EII}$ are acting) and the negative alternating–current feedback (only R_{EII} is acting) can be selected independently of each other.

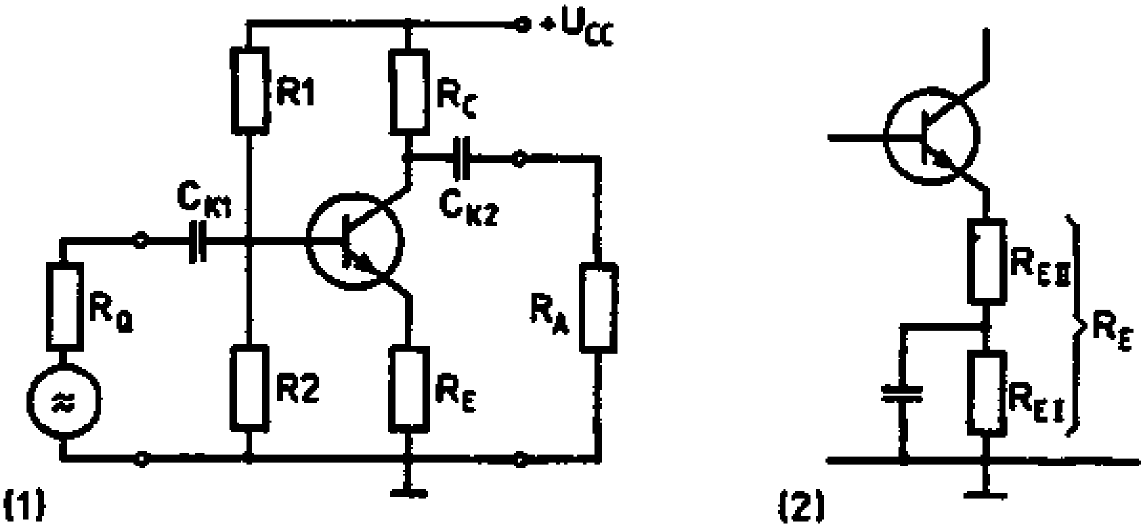


Figure 70 Negative current feedback in an emitter circuit

(1) basic circuit,
(2) modified circuit (part of circuit)

The negative current feedback causes the following changes of the service parameters of the transistor:

– The current gain remains more or less constant:

v'_{iTr} ? v_{iTr}

– The voltage gain is reduced and stabilized:

$$v'_u \approx \frac{v_u}{1 + k_u\, v_u} = \frac{v_u}{g_u}$$

$$k_u \approx \frac{R_L}{R_E} \text{ or}$$

$$k_u \approx \frac{1}{v_u} - \frac{1}{v_u}$$

– The input resistance is increased

$z_{1'}$? $z_1\, g_u$

– The output resistance is increased

$z_{2'}$? $z_2\, g_u$

Considering its stabilizing effect on the voltage gain, the negative current feedback as mainly utilized for voltage amplifiers.

The negative current feedback is shown here is effective only if the transistor is fed from a low−resistance signal source. Here, the following formula is to be applied:

$R_Q << Z'$.

Negative voltage feedback

The negative voltage feedback is characterized by the connection of the base voltage divider (resistor R1) to the collector. The circuit shown effects both a negative D.C. voltage feedback (bias point stabilization) and a negative A.C. voltage feedback.

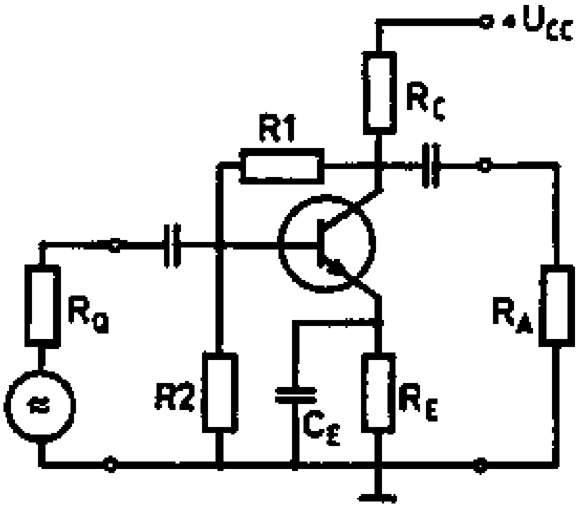


Figure 71 Negative voltage feedback in an emitter circuit

The negative A.C. voltage feedback causes the following changes of the service parameters of the transistor:

– The current gain is reduced and stabilized:

$$v_i' \approx \frac{v_i}{1 + k_1 v_i} = \frac{v_i}{g_i}$$

$$k_i \approx \frac{R_L}{R_1} \text{ or}$$

$$k_i \approx \frac{1}{v_i} - \frac{1}{v_i}$$

– The voltage gain remains more or less constant

$v_{u'}$? v_u

– The input resistance is reduced

$$Z_1' \approx \frac{Z_1}{g_i}$$

– The output resistance is reduced

$$Z_2' \approx \frac{Z_2}{g_i}$$

The negative voltage feedback as shown in this circuit is effective only if the signal source is a high−resistance one.

$R_G >> Z_1'$

$R_G = R_B // R_Q$

1.4.4. Operational amplifiers

In the case of the amplifiers so far under consideration, the amplifying stage was blocked by coupling capacitors at its input and its output. This permitted to connect signal generators or loads featuring a D.C. potential at their terminals. Such D.C. share did not change the bias point. But, on the other hand, these capacitors make the circuits unsuitable for amplifying such direct voltages as are frequent particularly in automation engineering.

In addition to that it is difficult to amplify signals of very low frequency because the capacitance of the coupling capacitors must become very high. This is why direct−voltage or direct−current amplifiers are of great technological importance.

The transmission of D.C. quantities requires the individual stages to be directly coupled. This is called a "galvanic coupling".

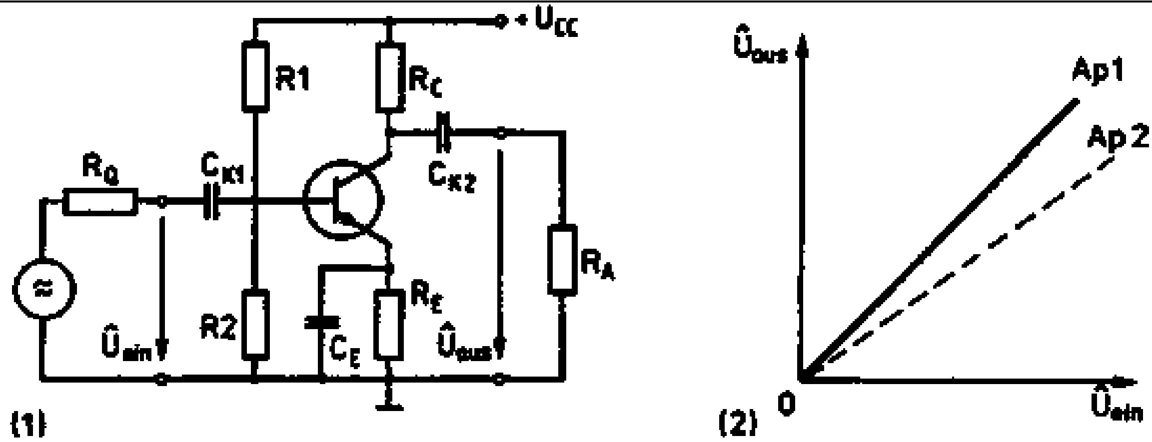


Figure 72 Resistance−capacitance coupling

(1) type of connection (RC elements marked in red),
(2) effect of a bias point displacement

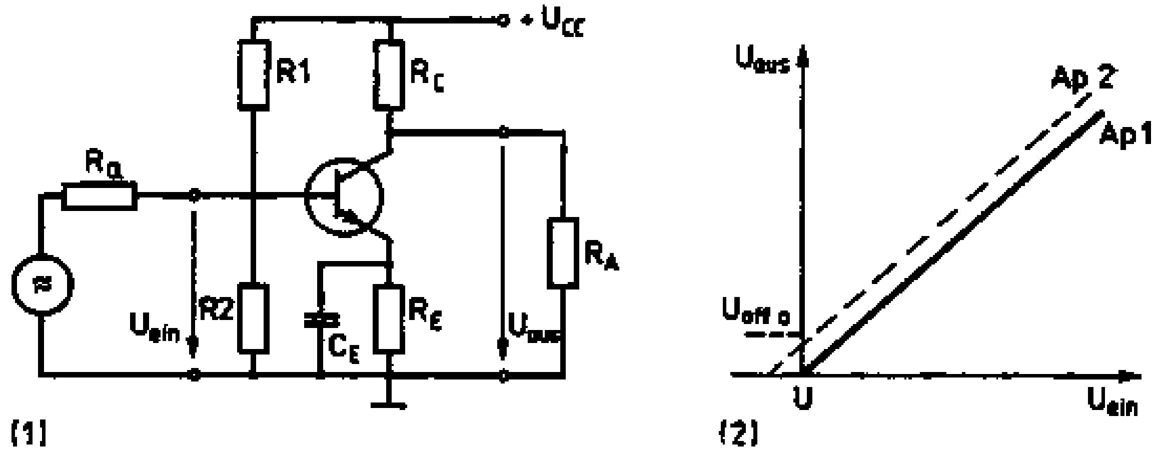


Figure 73 Galvanic coupling

(1) type of connection (galvanic coupling marked in red),
(2) effect of a bias point displacement

While in the case of the usual RC coupling by means of coupling capacitors (Figure 72) a bias point displacement becomes apparent as variation in gain only, a bias point displacement with a galvanic coupling (Figure 73) implies a modification of the output quantity, thus acting like an input signal.

This produces an output voltage even if there is no input signal. Such output voltage is called output offset voltage U_{offa}. To keep this voltage low, special circuits (differential amplifiers) were developed or the bias points were stabilized at considerable expense.

Only the development of integrated circuits made it possible to produce stable direct−voltage or direct−current amplifiers. Such integrated amplifiers are called operational amplifiers because they were used first in analogue computers for making calculations.

An operational amplifier is a functional unit permitting a stable amplification of D.C. quantities.

Its outstanding properties are due to

- the differential amplifier principle being utilized,
- close thermal coupling of all components that are arranged on a chip,
- high open−loop gain permitting a strong negative feedback.

A differential amplifying stage consists of two standard amplifying stages, the transistors of which are coupled by emitters. Consequently, both base terminals become empty and can be driven by signals. But, due to the emitter coupling, only the difference of the signal voltages at the two inputs is amplified. For this reason, this type of amplifier was called "differential amplifier".

A largely symmetrical arrangement of the two amplifier halves contributes to increasing the circuit effect. Such symmetrical arrangement can be implemented more easily with circuits. Figure 74 shows the basic circuits of a differential amplifier.

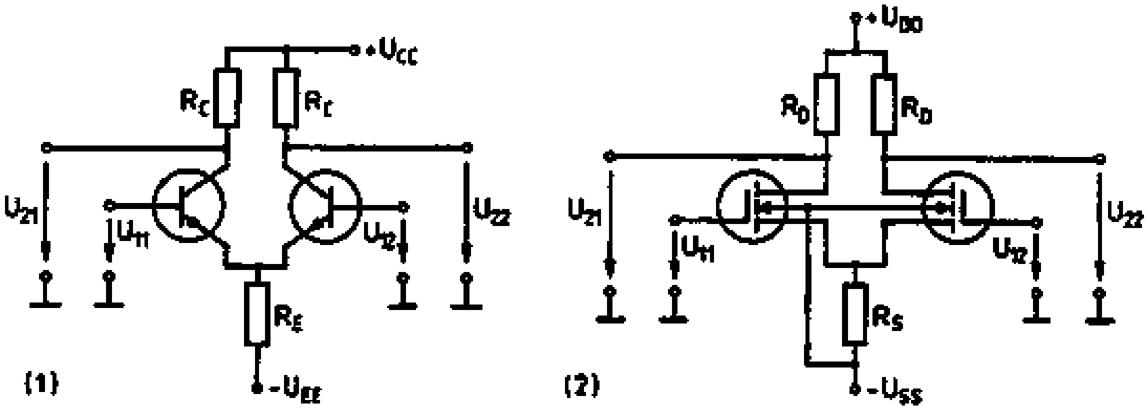


Figure 74 Basic circuit of a differential amplifier

(1) with bipolar npn transistors,
(2) with unipolar n−channel MOSFET (depletion type)

U_{11} input voltage of the 1st transistor
U_{12} input voltage of the 2nd transistor
U_{21} output voltage of the 1st transistor
U_{22} output voltage of the 2nd transistor

In unmodulated condition (in quiescent state), half of the current fed via R_E and R_S, respectively, passes through each transistor. This quiescent state is disturbed by modulation; the current distribution changes and various output voltages emerge. Referring to modulation, we distinguish the differential modulation $U_{11} = -U_{12}$

and the common−mode modulation $U_{11} = U_{12}$.

$U_{11} = U_{12}$. can be both D.C. and A.C. voltages ($U_{11} = \hat{U}_{11}$ and $U_{12} = \hat{U}_{12}$).

As to a differential modulation (Figure 75) the following formulas apply:

$$v_{uD} = \frac{U_{22} - U_{21}}{U_D} \approx \frac{R_C I_{EA}}{U_T} = \frac{R_C}{r_d}$$

$U_D = U_{11} - U_{12}$ (when entering the voltages heed the signs) or

$$v_{uD*} = \frac{U_{22}}{U_D} = -\frac{U_{21}}{U_D} = \frac{v_{uD}}{2}.$$

v_{uD} signifies the balanced and v_{uD*} the unbalanced voltage amplification.

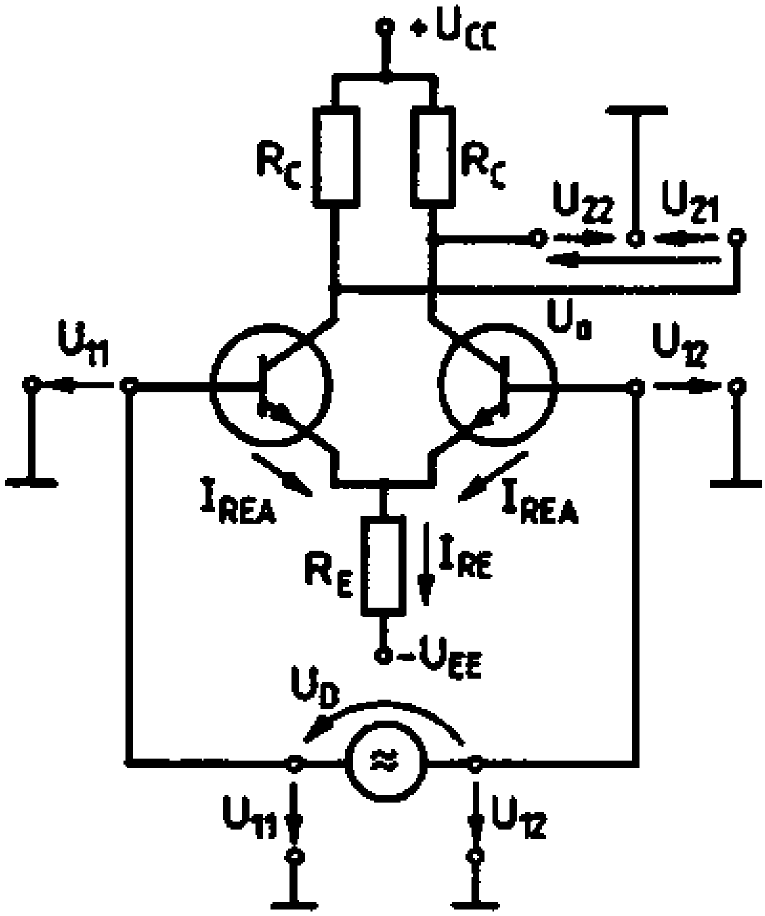


Figure 75 Voltage and current relations in the case of differential modulation

In general, we speak of balanced voltages when, related to earth, $U_1 = -U_2$.

Both voltages, better referred to as potentials here, are balanced to earth. The transmission is to be made through two lines, both of which must feature a potential to earth. They are earth−free.

As far as an unbalanced voltage is concerned, the value of one potential is zero. The transmission is to be made through two lines, one of which is applied to earth potential.

Consequently, the voltages U_{11}, U_{12}, U_{21}, U_{22} are unbalanced, while the voltages U_D and U_a are balanced.

As to a common−mode modulation (Figure 76) the following formula is applicable:

$$v_{uG*} = \frac{U_{21}}{U_G} = \frac{U_{22}}{U_G} = \frac{R_C}{2\ R_E}.$$

In Figure 76, the emitter resistance has been distributed among the transistors.

2 R_E are acting for each transistor. Passing through this resistor is $I_{EA} = I_{RE}/2$. Here, the same partial voltage arises as if I_{RE} was passing through R_E. A symmetrical line is drawn into the circuit, since consideration of

either half will do. Supposed the circuit is symmetrical throughout, the gain for a balanced output voltage must become v = 0, because in such event U_{21} is always equal to U_{22}. In a circuit this cannot be implemented, however.

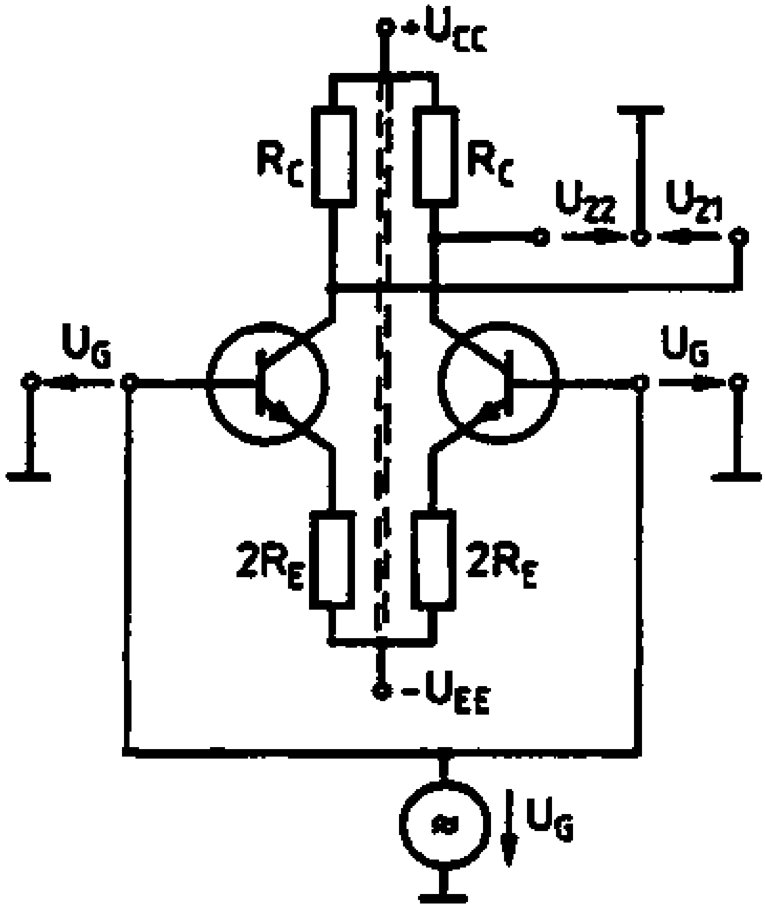


Figure 76 Voltage and current relations in the case of common−mode modulation

By keeping the value of R_E high, v_{uD} * >> v_{uG} * is being aimed at. The ratio

$$G = \frac{V_{ud^*}}{V_{uG^*}} = \frac{2\,R_E}{r_d}$$

is called common−mode rejection ratio. With operational amplifiers, the common−mode rejection ratio reaches values ranging between 10^3 and 10^5 (10...100 dB).

Thus, the common−mode rejection ratio indicates how many times a differential signal is amplified.

Variations in the working voltage and ambient temperature are always acting simultaneously and equidirectionally on both the transistors of the differential amplifier, thus being common−mode signals. A strong common−mode rejection, therefore, implies a high immunity towards such variations.

R_E cannot be too high, however, since this would make the amount of the direct voltage 2 I_{EA} R_E too high and render the supply of − U_{EE} uneconomical. For this reason, R_E is replaced by a constant−current source, which, equipped with discrete components, designed as emitter stage of negative current feedback and in circuits as current image.

The basic circuit of a constant−current source is shown in Figure 77. The base potential is stabilized by the z−diode V2. The output current is stabilized by means of a negative current feedback through R_E.

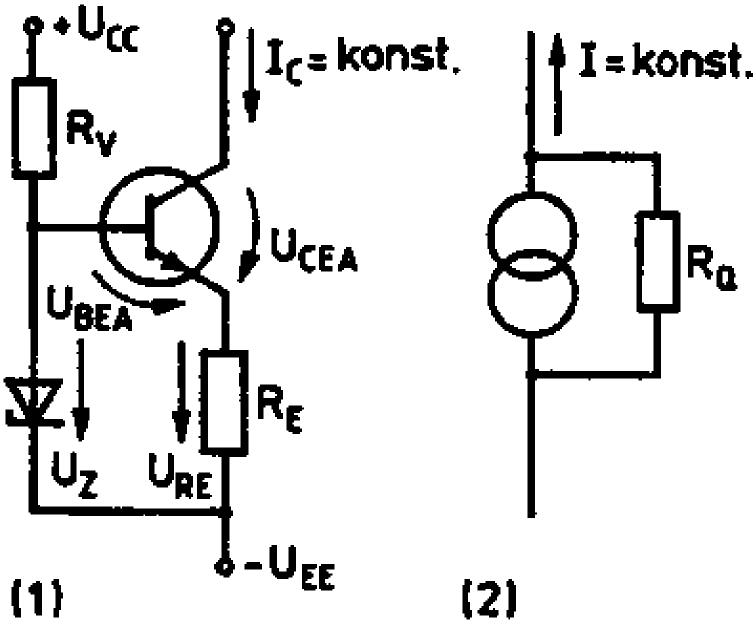


Figure 77 Basic circuit of a constant−current source with a bipolar transistor

(1) type of connection,
(2) symbol of a constant current source

Acting as D.C. internal resistance,

$$R_1 = \frac{U_{CEA} + U_{RE}}{I_C}$$

In the event of the current changing, the A.C. internal resistance (source resistance) becomes effective

$$R_Q \approx \frac{1}{h_{22e}}\left(1 + \frac{h_{21e} R_E}{R_E + h_{21e}\ r_d}\right).$$

As to equal transistors, the following is applicable:

$B_1 = B_2 = B$ and $I_{B1} = I_{B2} = I_B$.

Consequently, the current ratio becomes

$$\frac{I_2}{I_1} = \frac{B I_B}{I_B(B+2)} = \frac{B}{B+2} = S$$

$I_2 = SI_1$.

The image ratio S can become $S \begin{smallmatrix}>\\=\\<\end{smallmatrix} 1$, and reflected with S, the current I_1 appears as I_2. Integrated circuits often have a so−called <u>current bench</u> where various currents are derived (reflected) from a reference current I_1.

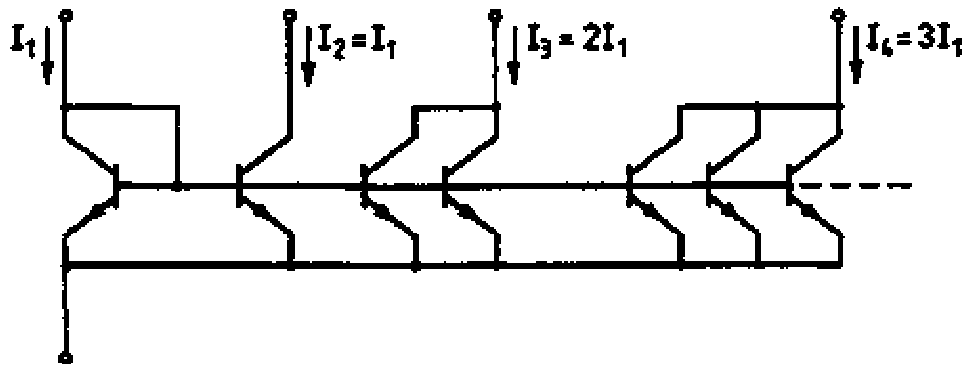


Figure 78 Schematic of a current bench

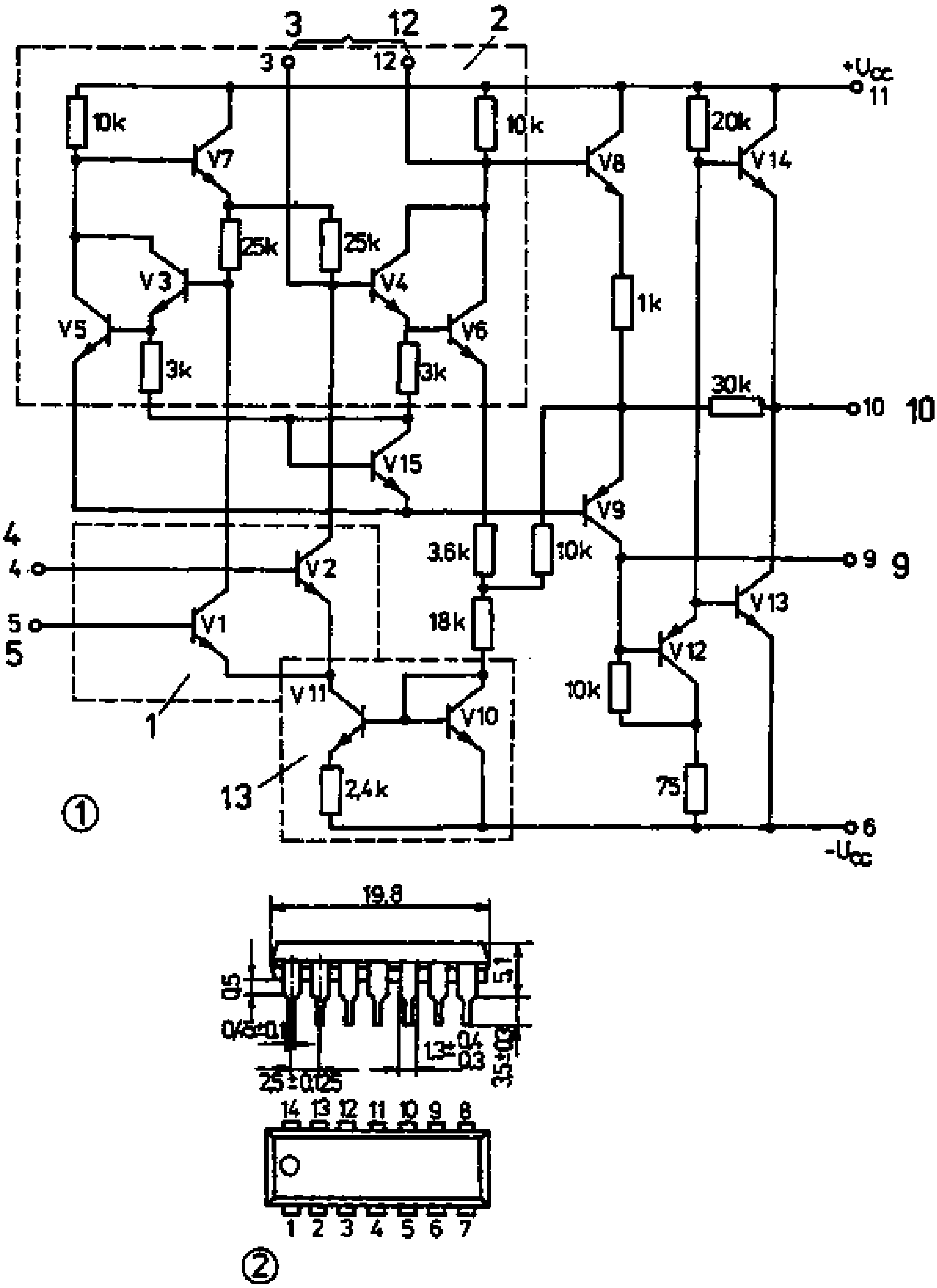


Figure 79 Operational amplification

(1) internal circuit,
(2) connections and dimensions
1 differential amplifier, 1, 2 differential amplifier 2, 4 inverting input, 5 non−inverting input, 3/12 input frequency compensation, 9 output frequency compensation, 10 output, 13 mirror image

Differential amplifiers and current images are standard subcircuits, which are often called substructures, of integrated analogue circuits. Let us demonstrate this by taking for example an operational amplifier, the internal circuit of which is represented in Figure 79. The differential amplifiers and current images are marked.

Looking at the circuit to Figure 79, you will notice transistors at several points that are interconnected without any further components (e.g. V3/V5 and V4/V6). This type of interconnection is called Darlington circuit. It can be produced by using transistors of equal or different sequences of zones (Figure 80). In this case, the following is applicable:

h_{11e} * ? 2 h_{111e} h_{212e} h_{11c} * ? h_{111e} + h_{211e} h_{112e}

h_{21e} * ? h_{211e} h_{212e} h_{21c} * ? – h_{211e} h_{212e}

h_{22e} * ? h_{222e} * h_{221e} h_{212e} h_{22c} * ? h_{222e} * h_{222e} h_{221e}

Of advantage is the high current amplification of a Darlington layout, that is essential, above all, for power transistors. Darlington transistors are produced, too, featuring two transistors which are interconnected as shown in the drawing and encapsulated in a housing. In the case of the complementary layout (Figure 80 (2)) the emitter of the transistor V2 acts as collector. By interchanging the sequences of zones it is possible to produce npn– and pnp–transistors.

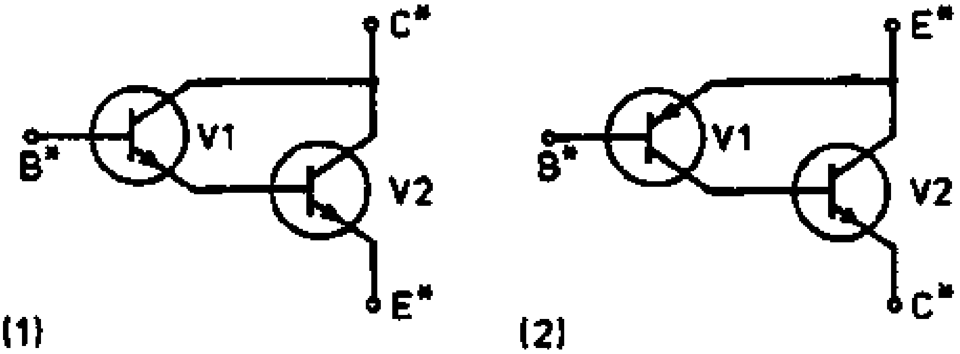


Figure 80 Darlington circuit

(1) standard (acting like a npn transistor),
(2) complementary (acting like a pnp transistor)

The indicated circuit details are important for the circuit since it is also possible to set them up with discrete components, except for the current image. For an operational amplifier (DV) they are of minor importance because, in order to use integrated circuits, you must have knowledge of their terminal details, but not of their internal circuit. In practice, we often assume an ideal DV which is characterized, last not least, by

– an infinite open–loop gain v_{uDO},
– an infinite common–mode rejection ratio,
– an infinite differential and common–mode resistance,
– an output resistance of zero,
– an infinite bandwidth (f_o ? ?).

Unless expressly stated, the ideal DV is always taken as basis. A comparison with the real values shows that the operational amplifiers actually in use come very close to these ideal values. The negative feedback, which is always being utilized, causes the ideal values to come still closer to the real zones.

A negative feedback is always to be conducted from the output to the inverting input. If not so, a positive feedback arises which brings about a self–excitation. In such case, the circuit will oscillate, i.e. there will be an A.C. voltage at the output, even without an input signal*

The input signal can be ded both to the inverting and to the non–inverting input. Consequently, we distinguish the following two basic circuits inverting amplifier (Figure 81 (1)), non–inverting amplifier (Figure 81 (2)).

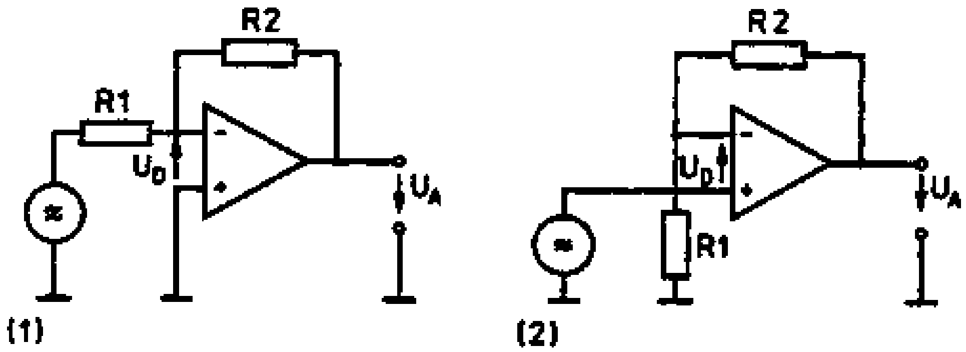


Figure 81 Basic circuits of an operational amplifier

(1) inverting,
(2) non−inverting

The amplification can be calculated for the ideal OV:

inverting amplifier

$$v_{uD\infty}' = -\frac{R_2}{R_1}$$

non−inverting amplifier

$$v_{uD\infty}' = 1 + \frac{R_2}{R_1}$$

The stroke with the formulas signifies the negative feedback. The condition of v_{uD} ? ? is not fulfilled in practice. For the real calculation of the amplification, therefore, the generalization mentioned hereinafter is more suitable. The input and output quantities are marked here by x_e and x_a, respectively. In practice, they can stand for a voltage or a current.

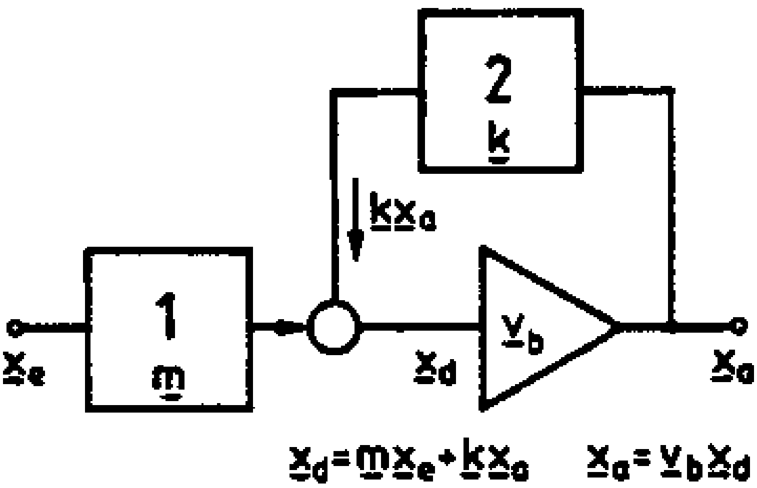


Figure 82 Calculation of the amplification of a wired operational amplifier

1 coupling,
2 back−coupling

Amplifiers are frequently used when there are low signal values. In such cases, however, disturbances become especially evident. Such disturbances include also the afore−mentioned offset parameters. In general, offset quantities refer to the input.

> The <u>input offset voltage</u> U_{offe} is that voltage which is to be applied to the input as differential voltage so as to obtain the output voltage U_a = 0V without signal.

The input offset voltage is caused by asymmetries. It strongly depends on the hardware, used and can assume positive or negative values.

Since the bases of the two input transistors of an 0V are free, the quiescent base current – which corresponds to I_{BA} with discrete, transistors – is to be fed and led off, respectively, through the external circuit. These quiescent currents are different, too.

The input offset current I_{offe} is the balance between the two quiescent base currents.

The manufacturers indicate a mean quiescent current I_B, which is also called BASE current.

The input offset current causes a differential voltage at the external resistors which superimposes the input offset voltage. When amplifying low D.C. values, therefore, an offset compensation must be effected by means of suitable external wiring. The circuits shown in Figure 83 can be used for offset compensation.

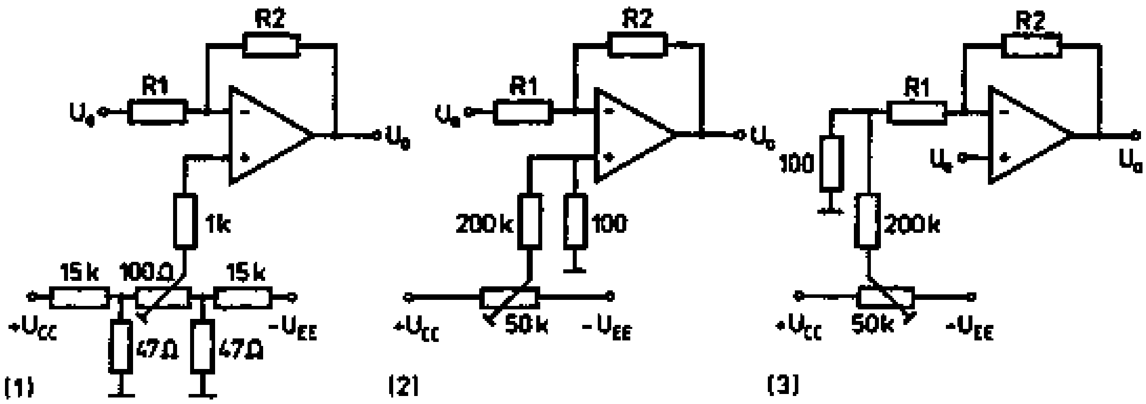


Figure 83 Offset compensation circuits

(1), (2) for inverting amplifiers,
(3) for non–inverting amplifiers

The offset values actually depend on the temperature, the operating voltage and the time. This dependence, which is called drift, cannot be eliminated by simple adjustment. The drift limits the accuracy when amplifying low values and the amount of amplification, as such.

Amplifiers for the amplification of very low direct voltages must feature an offset voltage drift, which is as small as possible. Amplifiers for the amplification of very low direct currents must feature a small offset current drift (and quiescent current drift, respectively).

Since the drift values are stated by the manufacturer of the 0V, such statement permits a selection which is suited to the respective application.

Operational amplifiers always consist of several stages (see Figure 79). In connection with external and internal capacitances – which can be e.g. the wiring capacitances that result from the technological layout of the circuit – these stages act as low passes. This means that the stage gain becomes smaller towards high frequencies. This gain decline is combined with a phase rotation of the signal. Upon performing a negative feedback, such phase rotation causes instabilities. In the event of the output signal additionally rotating by 180 deg. in phase, a feedback to the inverting input results in a positive feedback. When the loop gain amounts to > 1, then oscillations build up, which must be avoided by all means.

Nearly all operational amplifiers can be represented by a three–stage equivalent circuit.

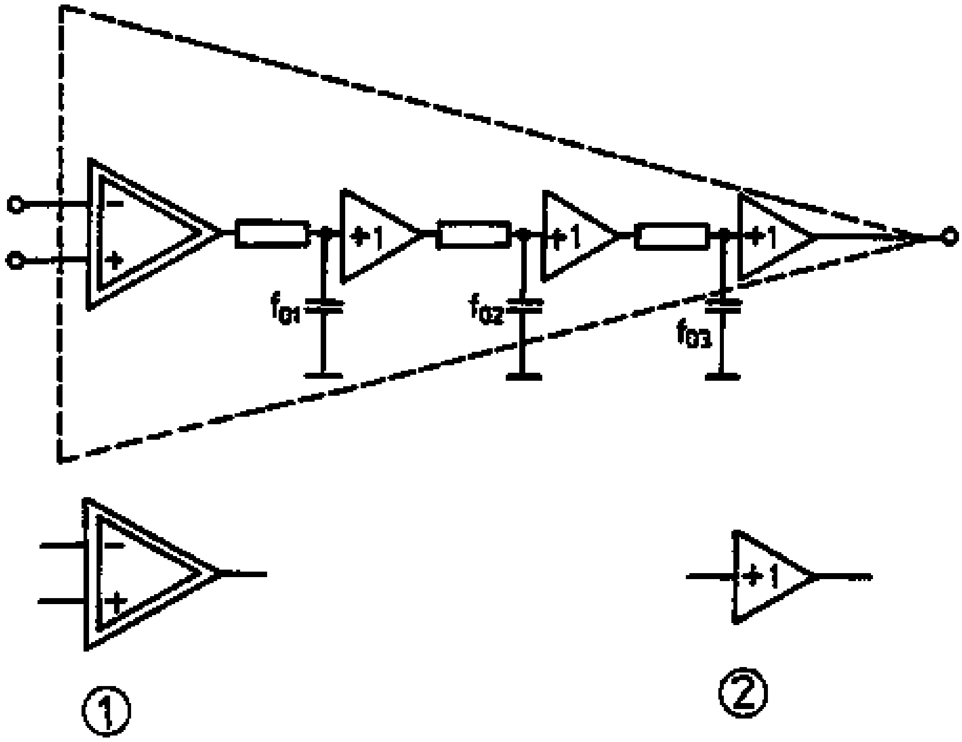


Figure 84 Model for the frequency dependence of amplification

(1) frequency−independent amplifier,
(2) ideal frequency−independent decoupling elements

From its very layout the circuit is designed so as to be able to apply $f_{01} << f_{02} << f_{03}$. On this condition, the amplitude characteristic and the phase characteristic take the course as shown in Figure 85. Let us explain this as follows:

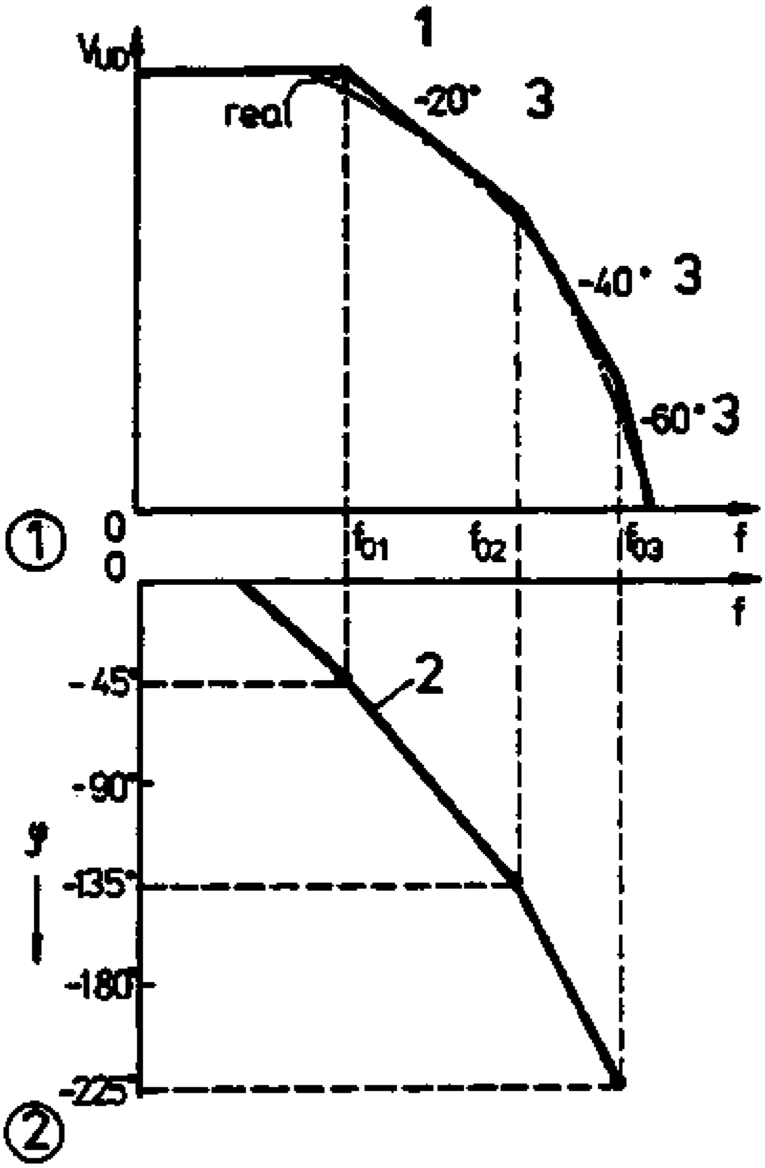


Figure 85 Frequency−response characteristics of an operational amplifier

(1) amplitude characteristic
(2) phase characteristic
1 idealized
2 idealized curve, 4dB per decade

At the frequency f_{01} the phase rotation has a value of $?_1$ = – 45 deg. in the first position; the amplitude decline is −3 dB and continues to decline at a rate of −20 dB per decade. When the frequency f_{02} is reached, a phase rotation of $?_2$ = – 45 deg. is effected in that position. But the position f_{01} already features $?_1$ = −90 deg. Adding up the two angles (phase angles of stages connected in chains are always added up), we come to $?_{1/2}$ = −135 deg. At f_{03} the second stage, too, features a phase rotation of $?_2$ = −90 deg. Adding the −90 degrees of the first stage and the −45 deg. of the third stage, (since its critical frequency has been reached), the sum amounts to $?_{1/2/3}$ = – 225 deg. Somewhere between f_{02} and f_{03} a value of $?_{1/2/3}$ = −180 deg. was reached. The frequency at which this phase angle arises was marked "f_{kr}" in Figure 85.

By means of an external wiring (frequency response correction), the user has to make sure that the additional phase rotation of $?_{1/2/3}$ < −180 deg. is maintained for the selected gain $v_{uD'}$. In practice, a safety zone – a phase margin – of +45 deg. is selected.

With that frequency which features an additional phase rotation of ? = −135 degrees, the loop gain must be of $vs = 1 \hat{=} 0\,dB$ only.

The necessary external wiring of the 0V terminals for frequency response correction is stated by the manufacturers. The values are shown in the below table. The wiring for this circuit is shown in Figure 86. The figures at the terminals indicate the pin number.

Table 6 Values for the components of the frequency−response compensation of an operational amplifier

V_D' dB	C_{K1} pF	C_{K2} pF	R_K k?
60	10	3	–
50	27	3	1.5
40	100	3	
30	270	10	
20	470	20	
10	2700	100	
0	4700	200	

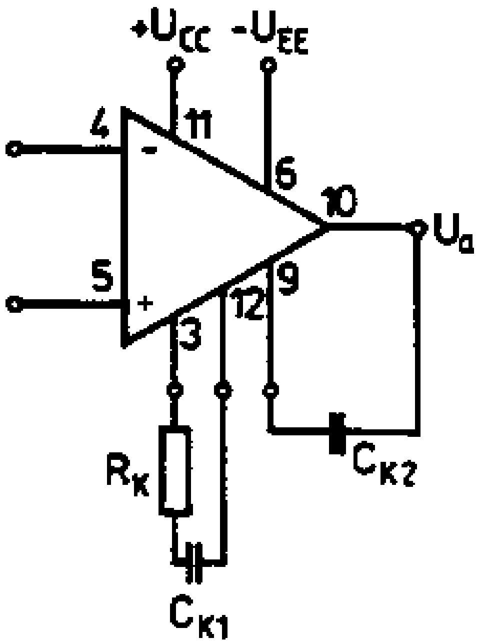
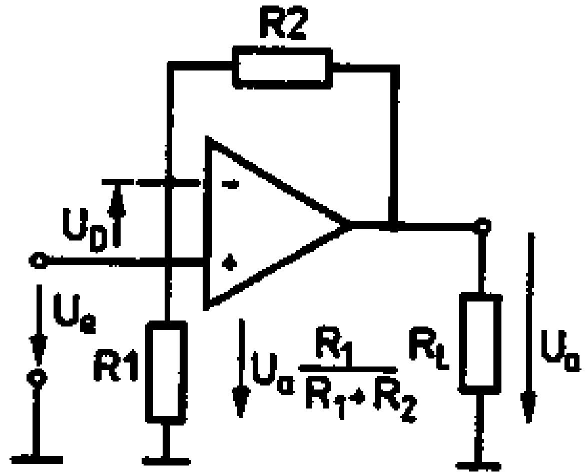


Figure 86 Wiring of an operational amplifier for frequency−response correction

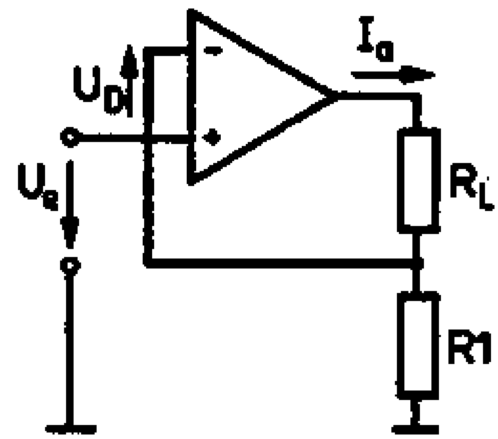
The reason why the operational amplifier is of such an importance to automation engineering is that its behaviour depends exclusively on the type of negative feedback. Designating a negative feedback, the first word signifies the type of the negative feedback while the second word signifies the output quantity from which the quantity fed back was derived. By selection of the negative feedback type it is possible to adapt the 0V to various tasks. This becomes evident from the gain definition which can be gathered from Figures 87 to 90.



$$U_D = U_e - U_a \frac{R_1}{R_1 + R_2}$$

$$v'_{UD\infty} = \frac{U_a}{U_e} = 1 + \frac{R_2}{R_1}$$

Figure 87 Negative voltage−voltage feedback



$$U_D = U_e - I_a R_1$$

$$v'_{D\infty} = \frac{I_a}{U_e} = \frac{1}{R_1}$$

Figure 88 Negative voltage−current feedback

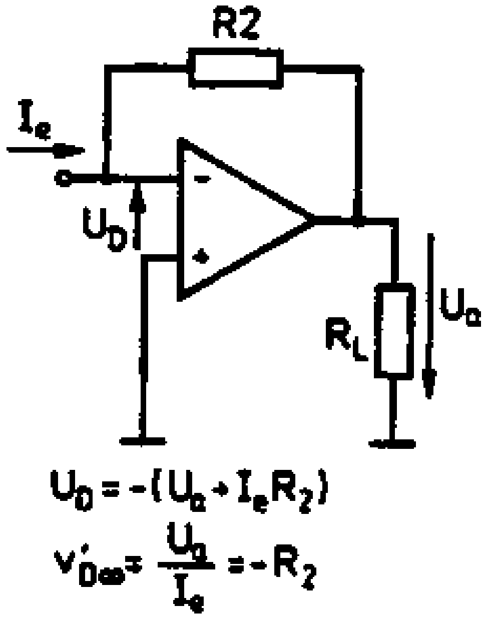


Figure 89 Negative current−voltage feedback

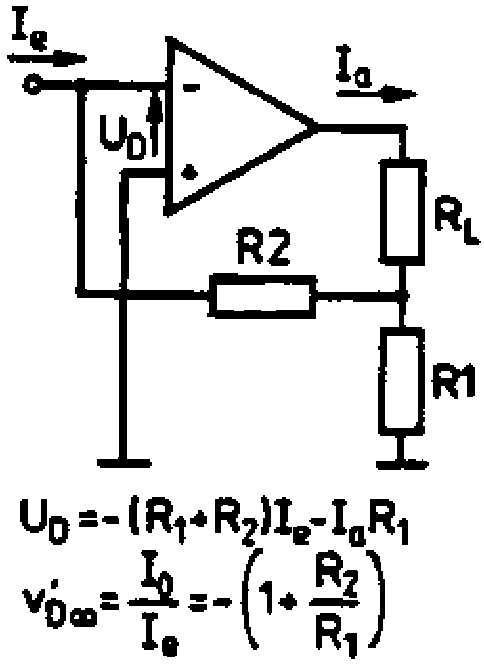


Figure 90 Negative current−current feedback

Table 7 Negative feedback circuits of operational amplifiers

Type of negative feedback	Type of amplifier	Ideal amplification	Operating amplification	Negative feedback factor	Input resistance (v_uDO = ?)	Output resistance (v_uDO = ?)
Negative voltage−voltage feedback	Voltage amplifier	$v_D' = 1 + \frac{R_2}{R_1}$	$v_b = \frac{U_a}{U_D}$ $v_b = v_{uDO}\frac{R_L // R_2}{r_a + R_L // R_2}$	$k = \frac{R_1}{R_1 + R_2}$	?	0
Negative voltage−current feedback	Voltage−current amplifier	$v_D' = \frac{1}{R_1}$	$v_b = \frac{-I_a}{U_D}$ $= \frac{v_{uDO}}{r_a + R_L + R_1}$	$k = -R_1$	?	?

Negative current–voltage feedback	Current–voltage amplifier	$v_D' = -R_2$	$v_b = \frac{U_a}{U_D} = v_{uDO} \frac{R_2}{R_L + r_a}$	$k = -1$	0	
Negative current–current feedback	Current amplifier	$v_D' = -\left(1 + \frac{R_2}{R_1}\right)$	$v_b = \frac{I_a}{I_e} = \frac{v_{uDO}}{r_a + R_L + R_1 // R_2}$	$k = -R_1$	0	

r_a output resistance of operational amplifier

Table 7 contains a comparison of the four negative–feedback basic circuits.

Consequently, an obvious thing to do is to use the voltage current negative feedback with U/I converters or the current/ voltage negative feedback with I/U converters. A suitable layout permits such circuits also to be used as system converters for the standard signal ranges*

1.4.5. Power amplifiers

Whenever the load resistance R_A of an amplifier requires a high power, a power amplifier is necessary. This is the case, for example, with nearly all servo units. Power amplifiers have an output power of 1 W < P_{out} < 1 kW. The last stage, the power output stage, of the power amplifier is of special importance. It directly feeds the load and decisively determines the properties of the complete amplifier. This is why the power amplifiers are also termed according to the circuit type of their power output stage.

The most essential criterion in this respect is the location of the bias point.

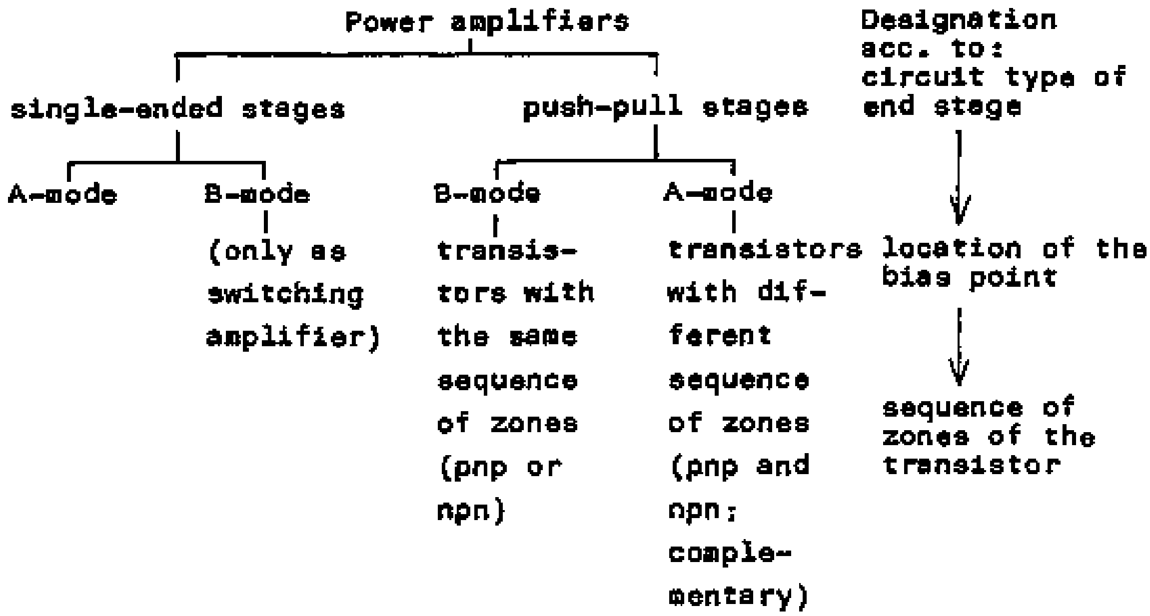


Table 8 Power amplifiers important to automation engineering

Unlike preamplifiers, which could be calculated by means of parameters typical of a transistor, a power amplifier cannot be calculated unless you know its specific family of characteristics. To achieve high powers, the transistors are to be modulated widely. If so, they act like a non–linear component. The characteristic parameters used with preamplifiers or voltage amplifiers, e.g. the h–parameters or the emitter diffusion resistance r_d (small–signal parameters), must not be employed here, any more.

The limits of modulation are represented in Figure 91 as well as the bias points, which are typical in automation engineering, were entered once more. The shown limits are those stated by the manufacturers.

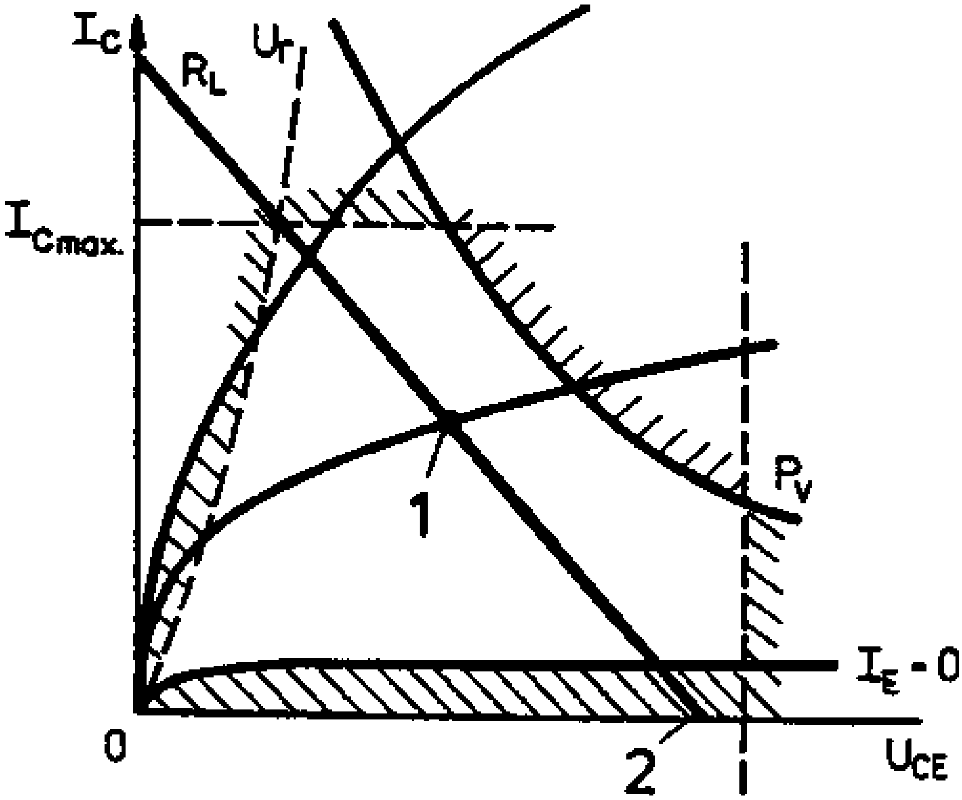


Figure 91 Modulation limits in the family of characteristics of a bipolar transistor

1 A−mode,
2 B−mode

Calculating a power stage, it is always supposed that a given power shall arise with a given load resistor R_A, e.g. 20 W with a resistance of 2 ?. Normally, the working voltage U_{CC} cannot be freely selected. In most cases it is determined by the plant or the appliance. A suitable circuit is, therefore, to ensure that the transistor is to be terminated (loaded) by its optimum load resistance $R_{L\ opt}$ which is available when two of the modulation limits, $U_{CE} = U_{CEmax} \cdot P_V = P_{Vmax}$ and $I_C = I_{Cmax}$, have been reached. In most cases you need transmitters for reaching these limits, since many a time R_A ? $R_{L\ opt}$. When transmitters shall be avoided, e.g. in the case of a wide−band transmission (language and music), you have to do without terminating by $R_{L\ opt}$ and, consequently, also without taking the maximum power possible.

Below is a consideration of the modes which depend on the bias point.

<u>A−mode</u>

The load resistor can be RC−coupled as usual for powers of up to P = 1 W or so (Figure 92 (1)). With higher powers, the losses at the R_C are too big. It is better to adapt the R_A through a transmitter (Figure 92 (2)) which is to be made so as to make

$R_L = R_L$ opt.

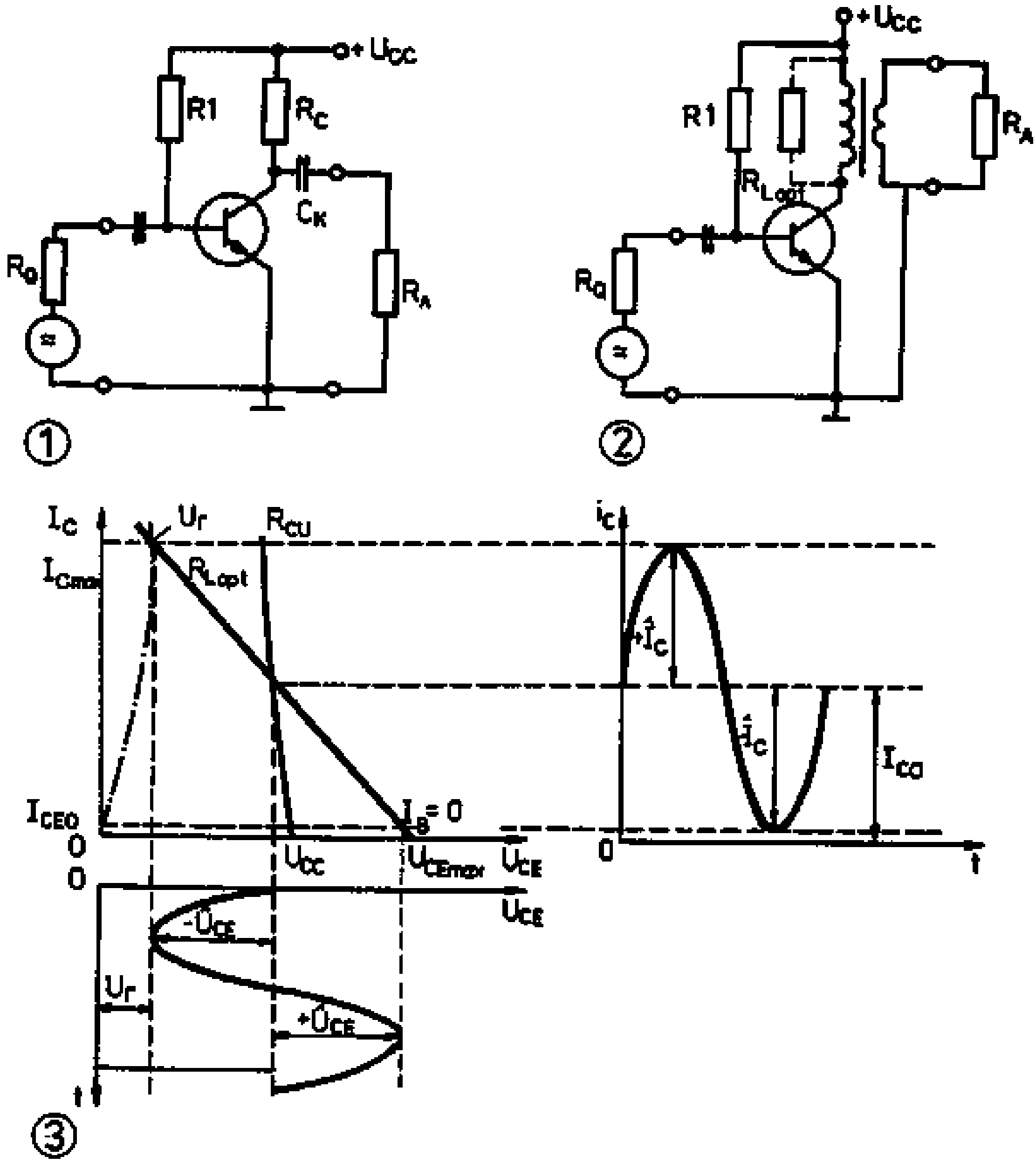


Figure 92 Single−ended A−mode amplifier in an emitter circuit

(1) with RC−coupling (for low powers only),
(2) with transformer coupling,
(3) modulation in the family of characteristics for transformer coupling;

R_{Cu} copper resistor of the transformer primary winding

You can read from Figure 92 (3):

$$R_{L\,opt} = \frac{U_{EE\,max} - U_r}{I_{C\,max} - I_{CEO}} \approx \frac{U_{CE\,max} - U_r}{I_{C\,max}} \approx \frac{2U_{CC} - U_r}{I_{Cmax}}$$

$I_{C\,max} >> I_{CEO}$ is considered in the approximation. The collector residual current I_{CEO} can be neglected with Si transistors in almost any case.

$$\hat{U}_{max} = \frac{U_{CE\,max} - U_r}{2} \left(\text{with} R_L = R_{L\,opt}\right)$$

$$\hat{I}_{max} = \frac{I_{C\,max} - I_{CEO}}{2} \approx \frac{I_{C\,max}}{2}$$

So the alternating power arising can be calculated. Before doing so, the modulation level m is introduced. With $(0 \le m \le 1)$ it is also possible then to cover a partial modulation or any modulation $(0 \le \hat{U} \le \hat{U}_{max})$ which corresponds to m ? 1.

$$\hat{U} = m \frac{U_{CEmax} - U_r}{2}$$

$$\hat{I} = m \frac{I_{C\ max}}{2}$$

On these conditions, the following is applicable to the alternating power arising on the load resistor R_L:

$$P_\sim = \frac{\hat{U}\hat{I}}{2} = \frac{m^2}{8}(U_{CE\ max} - U_r)\, I_{C\ max} = \frac{m^2(U_{CE\ max} - U_r)^2}{8R_L}$$

Also the D.C. power to be supplied by the battery can be calculated by means of Figure 92 (3)

$P_= = U_= I_=$

$$U_= \triangleq U_{ECA} = \frac{U_{CE\ max} + U_r}{2}\ U_{CC}$$

$$I \triangleq I_{CA} = \frac{I_{C\ max} - I_{CEO}}{2}\ \frac{I_{C\ max}}{2}$$

This makes

$$P_= = \frac{U_{CE\ max} + U_r}{2} \cdot \frac{I_{C\ max} - I_{CEO}}{2} \approx \frac{U_{CC} - 2U_r}{4}.$$

The equation for the efficiency

$$\eta = \frac{P_{out}}{P_{in}}$$

and the classification

$P_{out} = P_\sim$ and $P_{in} = P_=$

makes

$$\eta = \frac{P_\sim}{P_=} = \frac{m^2}{2}\frac{U_{CE\ max} - U_r}{U_{CE\ max} + U_r} \approx \frac{m^2}{2}\frac{U_{CC} - 2U_r}{U_{CC} + 2U_r}.$$

The transistor has a power loss.

$$P_V = P_= - P\ \frac{U_{CC} I_{C\ max}}{4} - \frac{m^2}{8}(U_{CC} - 2U_r) I_{Cmax}$$

The power loss reaches its maximum when there is no modulation at all (m = 0).

$$P_{Vmax} \approx \frac{U_{CC} I_{C\ max}}{4}$$

and its minimum with full modulation (m = 1).

$P_{v\,min}$? U_{CC} $I_{C\,max}$

In A−mode, with the modulation increasing, the power loss of a transistor is declining.

The power to be supplied by the battery or the power unit is constant in time. It is converted into heat at the transistor and at the load resistor. Without modulation, the transistor is loaded heaviest. It is able to transmit positive and negative signals.

B−mode

The Figures 93 (1) and (2) show the usual circuits for the non−ferrous and the transmitter−coupled designs. The location of the bias point permits to make a choice between the AB−mode (I_{CA}>0) and the B−mode (I_{CA} = 0). for automation engineering, the B−mode is more suitable when switching states are to be transmitted only.

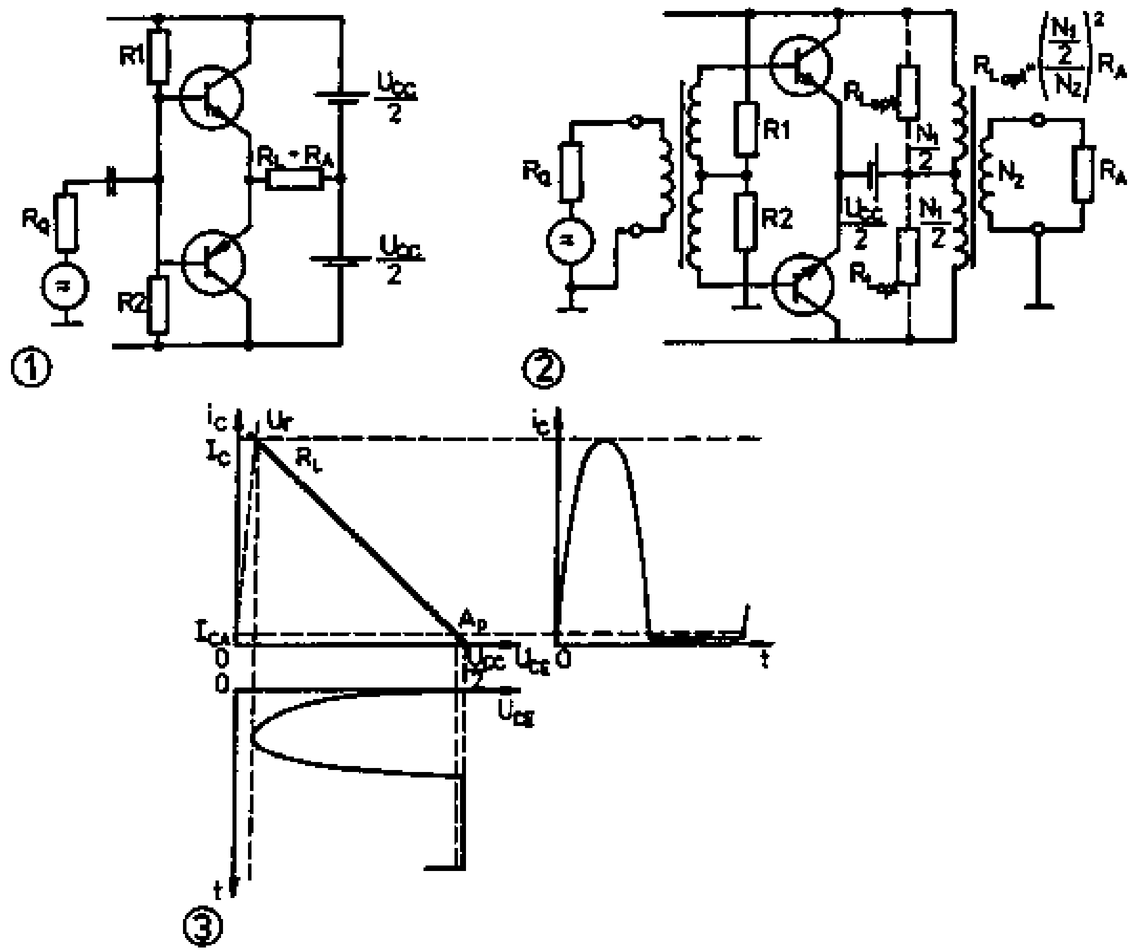


Figure 93 Push−pull AB−mode amplifier

(1) coreless with complementary transistors,
(2) with transformer coupling,
(3) modulation for a transistor in the family of characteristics (For I_{CA} = 0 the representations also apply to push−pull B−mode amplifiers)

The following equations apply also to be B−mode when I_{CA} is made zero. Because of the induced voltage in the output transmitter and the full control of the transistors in the circuit to Figure 93 (1), the following formula is always to be applied:

$$\frac{U_{CC}}{2} \leqq U_{CE\,max}.$$

Leaving the residual voltage out of consideration, consequently, the only limits in the family of characteristics still to be considered are P_{Vmax} and I_{Cmax}.

As shown in Figure 93 (3), modulation is effected in one direction only. For modulating in positive and negative direction two transistors are required which are modulated subsequently in time. These transistors must either feature different sequences of zones (complementary transistors; Figure 93 (1)) or, in the event of equal sequences of zones, be modulated through signals which are opposite in phase, such as are provided by the driver transmitter T1 in Figure 93 (2).

Contrary to the A−amplifier, the power loss of the transistor in unmodulated condition (quiescent power loss) is almost zero (AB−mode) or zero (B−mode). With modulation increasing, the power loss becomes higher and reaches its maximum at about 64% of the voltage modulation which corresponds to about 40% of the power modulation. In all, the states are more intricate than those of an A−amplifier. The basis for the following calculation instructions can be seen from Figure 93 (3).

$$R_L = \frac{\frac{U_{CC}}{2} = U_r}{I_{C1} - I_{CA}}$$

or for the B−mode ($I_{CA} = 0$)

$$R_L = \frac{\frac{U_{CC}}{2} = U_r}{I_{C1}}$$

In order to ensure a large modulation, $I_{C1} = I_{C\ max}$ is aimed at, with $I_{C\ max}$ representing the collector amperage limit admitted by the manufacturer.

The power loss in a transistor becomes

$$P_V = P_{=} - P_{\sim} \approx \frac{m}{\pi} \cdot \frac{U_{CC}}{2} \cdot I_{C\ max} - \frac{m^2}{4}\left(\frac{U_{CC}}{2} - U_r\right) \cdot I_{C\ max}$$

and depends on m, i.e. on the modulation.

Contrary to A−amplifiers, the power loss of the transistors of B− and AB−amplifiers gets higher with increasing modulation.

The values of the amperage or voltage which can be amplified by transistors are often not sufficient in automation engineering. Many servo units are operated from mains voltage. If so, thyristors are suitable as switches. Such circuit is called a quasi−continuous amplifier. Contrary to the amplifiers already described, where the signal was existing at any time (continuously), the signal is not always applied with a quasi−continuous amplifier. When the cycles "signal applied" and "signal not applied" are changed quickly enough, the amplifier, connected with integrating servo units, acts as if a continuous signal was applied. This is why it is called "quasi−continuous". Figure 94 illustrates the functioning of a thyristor as switch. In off−state the bias point is at Ap 1, the thyristor is high−resistive and acts like an open switch. An ignition pulse makes it conductive, the bias point hops to Ap 2, and the thyristor acts like a closed switch. When the holding point is passed, due to the anode current I and the anode voltage U_a being reduced, the thyristor is reset to Ap 1. With an alternating voltage applied, this cycle is effected automatically when the ignition pulses are synchronized with the mains frequency. Since the ignition power P_Z of a thyristor is considerably lower than the power P_L that can be switched in the anode circuit, there is a big power gain which justifies the term "amplifier".

$P_Z = U_z I_Z << P_L = U_L I_L$

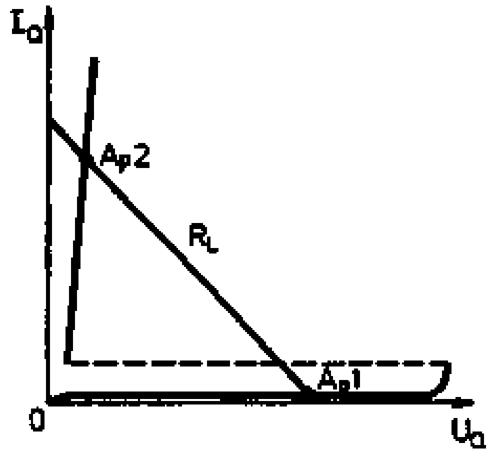


Figure 94 Functioning of a thyristor as switch

It is reasonable to consider the operating circuit and the ignition circuit separately.

The layout of the operating circuit strongly depends on the character of the load resistance. Load resistances often feature a great inductive element (motor, magnetic, drive, etc.) Then there are phase shifts between the current and the voltage which let the current become zero from time to time. This is called intermittent operation. Such intermittent operation is unfavourable because of surge−type forces in the load resistance. It can be avoided by an adequately high inductanceusing an additional coil L_z, if necessary − and a zero diode V2.

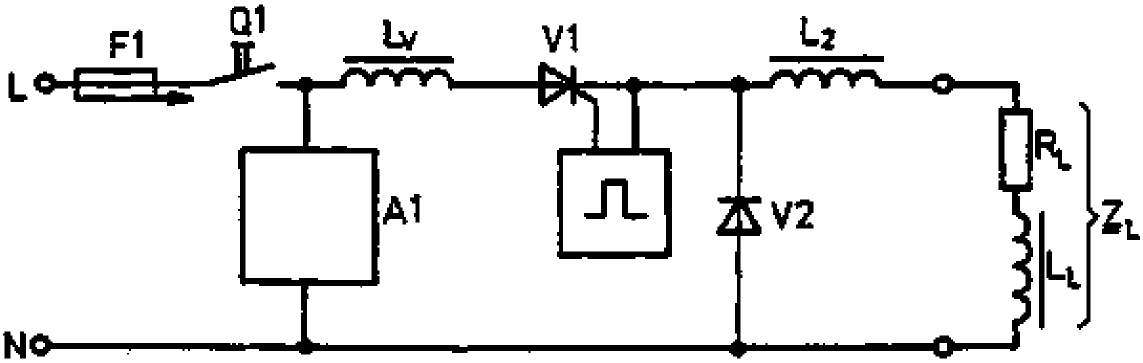


Figure 95 Basic layout of the operating circuit of a quasi−continuous amplifier

The coil L_V serves to diminish the radiation of highly frequent disturbances into the mains. In addition to that, this coil limits the rate of current rise di (?i)/dt ?t. The power switch Q1 is required to make the operating circuit dead. The blocked thyristor does not result in a dead state!

The quick−break fuse F1 serves as overcurrent protection, many a time high−speed fuses are also used. The functional unit A1 protects against overvoltages. Figure 96 shows a possible internal circuit for A1. In a rectifier bridge circuit a high−capacitance capacitor (C > 100 µF) acts as charge store.

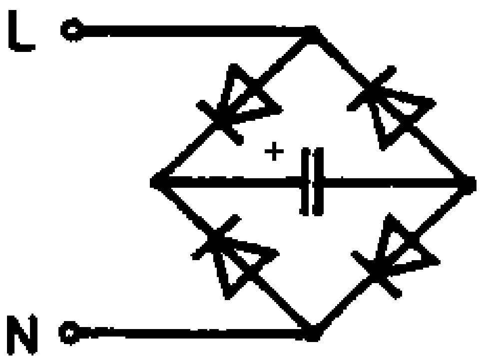


Figure 96 Overvoltage protection circuit

In addition to the load resistance, the ignition circuit is decisive for the variation with time of current and voltage. The ignition circuit provides the thyristor with pulses that are synchronized with the mains frequency. Apart from the form and the energy content of the ignition pulses, which must meet the conditions for a safe ignition of the thyristor, their time slot with respect to the voltage in the operating circuit and their time sequence are essential for the conditions in the operating circuit.

Thyristor circuits can be operated as

- switches
- phase−angle control
- oscillation block control.

When used as switch, the thyristor connects or disconnects the consumer (the load), if so required. Compared with mechanical switches it features the following advantages:

- No mechanically moved parts.
- Very short switching times.
- A very high switching frequency.

Its disadvantage is that, in a simple circuit, only one alternating current half−wave is connected through onto the consumer. This disadvantage is eliminated by operating the thyristor by means of a rectifier bridge circuit.

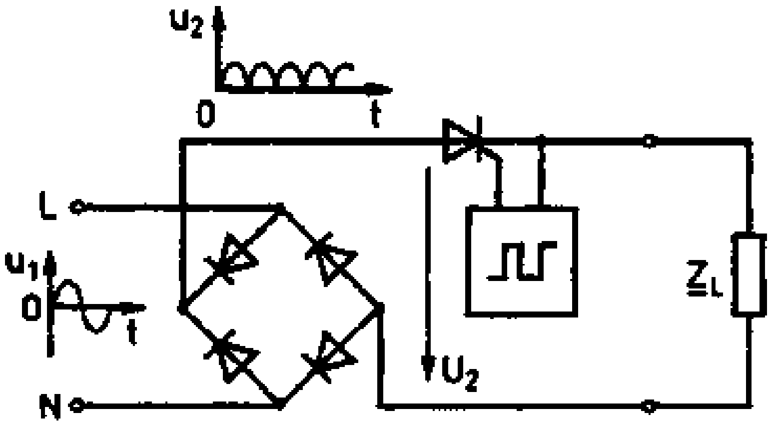


Figure 97 Additional rectifier bridge circuit for the use of a thyristor as switch

In this case, however, simultaneously a direct current is passing through the consumer. If this is inadmissible, a bidirectional triode thyristor (triac) is to be used. Instead of a pulse ignition a positive direct voltage can be used which ignites the thyristor at the beginning of each positive half−wave. Setting or control of the power conversion at the consumer is possible with the next mode only.

In the case of the <u>phase−angle control</u> the thyristor is ignited at a given time with respect to the zero passage of the alternating current in the operating circuit. The time sequence has already been mentioned when describing the thyristor. In the following, let us consider a simple layout for the ignition circuit of a bidirectional triode thyristor for phase−angle control.

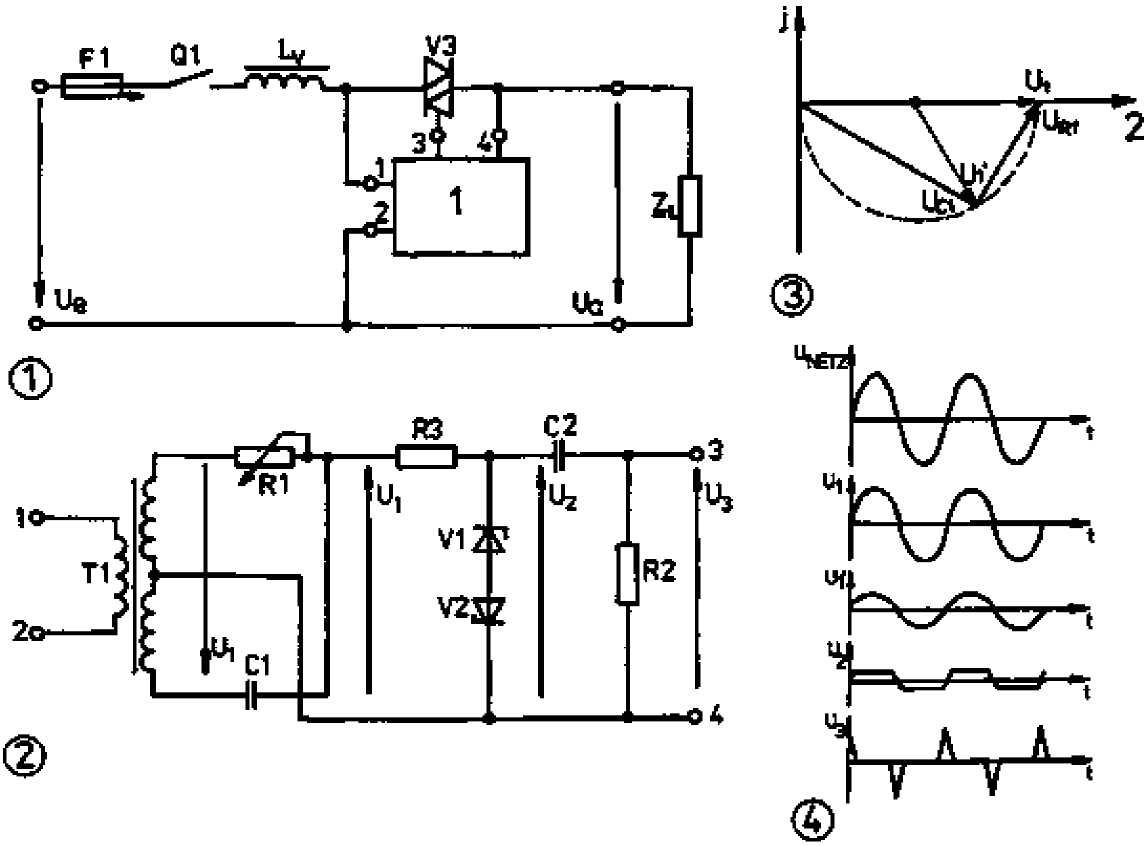


Figure 98 Phase−angle control with a bidirectional triode thyristor (triac)

(1) operating circuit,
(2) ignition circuit,
(3) vector diagram to explain the phase shift,
(4) line diagram of voltages (for about 90 degrees' phase shift)
1 ignition circuit,
2 real axis

The voltage U_1 with the transformer T1 (Figure 98 (2)) is divided into a voltage via C1 and another via R1. These two partial Voltages are always vertical upon each other, for U_{R1} is an active voltage and U_{C1} a reactive voltage. Consequently, their connecting point describes a semicircle in the vector diagram (theorem of Thales) (Figure 98 (3)). The voltage U_1, resulting therefrom is always $U_{1'} = U_{1/2}$, however its phase angle with respect to U_1 can be theoretically adjusted by 0 ... − 180 degrees, when R1 is modified between zero and infinite. Practically, it is possible to set from abt. −20 to −160 degrees. With

$$\frac{1}{\omega C_1} = R_1$$

a satisfactory linearity is achieved.

The voltage $U_{1'}$ is limited by means of two Z−diodes (in Figure 98 (2) V1 and V2) and the voltage U_2 is produced. On the condition that

$$C_2 \cdot R_2 = \frac{1}{10\ f_{mains}} = \frac{1}{10.50\,\mathrm{Hz}} = \frac{1}{0.5.10^3\ \frac{1}{s}} = 2 \cdot 10^{-3}\,s = 2ms$$

needle−type pulses arise in a subsequently arranged differentiating element. These needle−type pulses serve to trigger the bidirectional triode thyristor V3 (Figure 98 (1)). It is able to process both positive and negative ignition pulses and, therefore, ignites with a phase shift set at R1 in each half−wave. As far as Figure 98 is concerned, a value of about −90 degrees was selected.

In this circuit R1 is at mains potential over the bidirectional triode thyristor. This may cause accidents!

A phase−angle control causes heavy harmonics when igniting the thyristor outside the zero passage, which alter the form of mains voltage and cause high−frequency interferences. This type of control, therefore, is more and more replaced by the oscillation block control.

In the case of the oscillation block control, the consumer is always fed with full periods of the mains A.C. voltage.

Power setting or control is effected through the number of periods per oscillation block. This mode is particularly suited to integrating consumers bridging the dead time, such as heaters and motors. Because of the flickering it is not possible to set the brightness of incandescent or fluorescent lamps. The ignition of the thyristor in the zero passage of the voltage curve offers a specific advantage.

An integrated circuit includes the sophisticated electronics circuit of the ignition circuit. This circuit contains all modules necessary to perform switching operations, phase−angle control or oscillation block control with ignition of the thyristors in the zero passage of voltage or current. Figure 99 represents a general wiring diagram of a circuit.

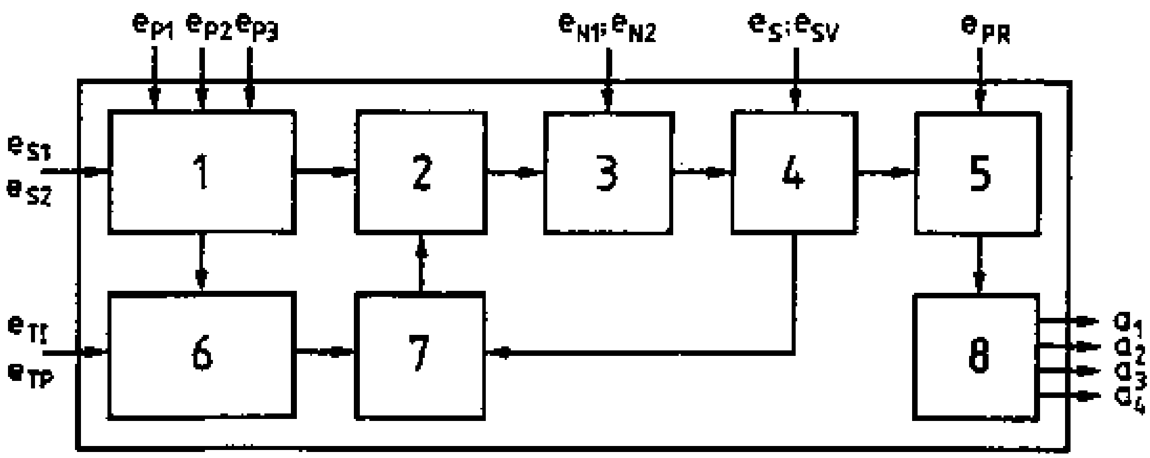


Figure 99 General circuit layout

1 synchronization logic,
2 channel change−over,
3 pulse mixing
4 pulse gate,
5 inverting control,
6 control input,
7 ignition pulse formation,
8 output driver

1.4.6. Sine−wave oscillators

Sine−wave oscillators are functional units which convert a direct−current power into a sine−type alternating−current power.

The output voltage is generated in the functional unit. For this reason it is often called "generator", too. Sine−wave oscillators are important to automation engineering when measuring values are to be transmitted over longer distances or when the frequency itself is the signal parameter. In the first case We speak of a carrier process. the measuring value is modulated upon an easy−to−transmit high−frequency carrier oscillation. In the latter case we speak of frequency modulation which is particularly resistant to interferences. But, on the other hand, modulation and demodulation are more expensive than in the case of an amplitude modulation.

Consequently, the most important requirements with respect to sine−wave oscillators are

− the frequency height
− the frequency stability in the event of temperature and operating voltage fluctuations

– a frequency drift upon aging of the components
– the form and stability of the amplitude.

Being of particular importance, the frequency and amplitude stability is an essential criterion for the quality. In the range between f ? 1 and 10^5 Hz, sine oscillations are generated by RC oscillators, while in the range between f ? 10^5 and 10^9 Hz they are generated by LC oscillators. The generation is based on the feedback principle, to be more specific on the positive feedback principle.

A range of up to some hundreds of kilohertz is usual for automation engineering purposes.

<u>Positive feedback principle</u>

In the equation $v' = \frac{v}{1 - v\,k}\,v'$ becomes ? when vk becomes v = 1. This state is called <u>self–excitation condition</u>. v k = 1,

i.e. the

– amplitude condition / v k / =1
– phase condition ?v = ?k = 0

must have been met. This can also be explained by way of physics:

An oscillation cannot be maintained unless

– so much energy is fed back to the input that all losses arising in the feedback loop are compensated (amplitude condition)

and

– the phase position of that energy is such that the energy fed back adds up to the input energy (phase condition).

Consequently, the condition v k = 1 describes the steady state. If an oscillation is to build up, the condition is:

|k v| > 1.

Then, a regulating circuit is to regulate the loop gain to 1 which is to be kept constant. For this purpose, often an amplitude–dependent shift of the bias point into a range having a smaller gain is utilized.

The inductive coupling principle represented in Figure 100 is frequently applied.

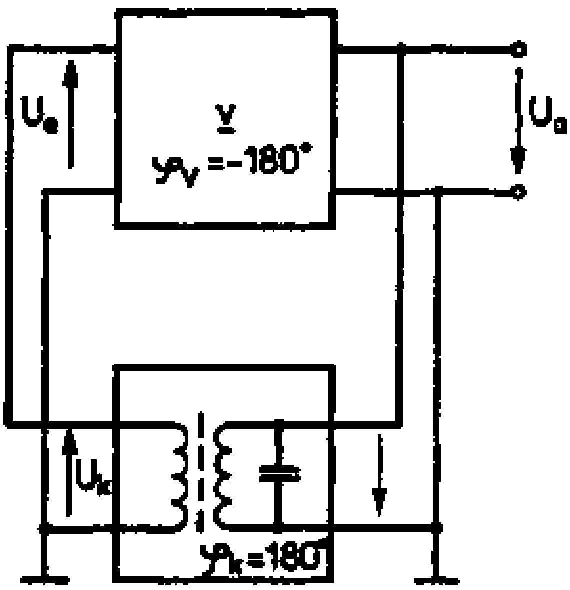


Figure 100 Schematic of inductive positive coupling

On the condition of a phase shift in the amplifier of ? v = −180 deg., as is caused e.g. by a normal emitter stage, the transformer, too, is to feature a phase shift of ? k = 180 deg.

The amplitude condition can be fulfilled by selection of the transformer voltage ratio.

This principle is applied with the circuit of a Meissner oscillator (Figure 101).

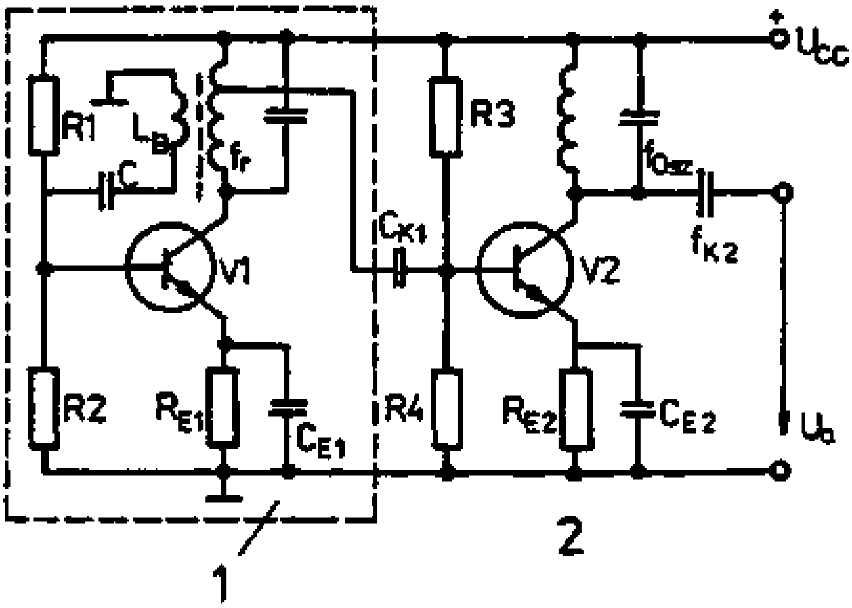


Figure 101 Meissner oscillator with separator stage

1 oscillator stage
2 separator stage

The transistor V1 has the normal wiring for stabilizing the bias point (R1; R2; R_{E1}). The voltage arising with the oscillating circuit is fed back to the base via the coil L_B and the capacitor C. When the amplitude and phase conditions are fulfilled, an oscillation is built up with f_{osz} ? f_r provided that k v > 1 in the starting state of oscillations. Consequently, the bias point is to be selected so as to let k v become > 1 (AB−mode). With the oscillation amplitude increasing, the oscillation is rectified at the curved input characteristic. This causes, among other things, a direct current, which charges the capacitors C and C_E so as to adjust the bias point towards the B−mode direction.

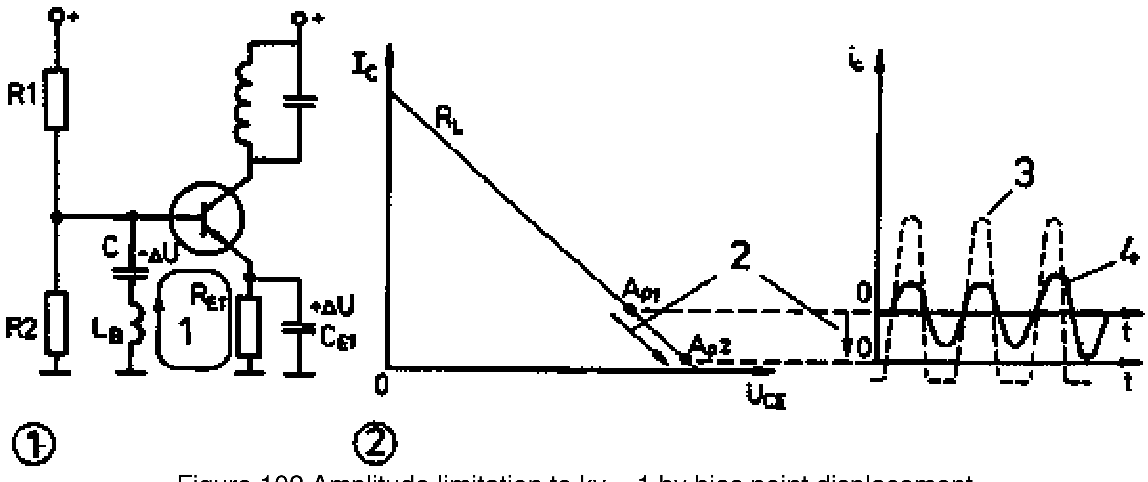


Figure 102 Amplitude limitation to kv = 1 by bias point displacement

(1) current behaviour in the circuit,
(2) representation in the family of characteristics
1 direction of current,
2 effect of limitation,
3 big amplitude /kV/= 1.4 small amplitude /kV/ 1

In this connection, the gain v declines and k v becomes equal to 1. This value is automatically maintained, because

$U_{BE} = -\ (?U_{CE} + ?U_C)$.

The collector current is not sine−type any more, the oscillating circuit is just impulsed by it, it continues to oscillate freely and thus generates a pure sine voltage.

This voltage is coupled out via C_{K1} (Figure 101) and fed to a separator stage which can also be designed as collector stage, thus facilitating decoupling of low load resistances.

RC oscillators

For low frequencies, the values for L and C of the oscillating circuit get big, the components get bulky and heavy. Taking this into account, RC circuits are used in such cases. From the wide variety of circuits having resistors and capacitors, such circuits are suitable only which shift the phase by 180 deg. or 0 deg. In connection with amplifiers also causing phase shifts of 180 deg. and 0 deg., respectively, circuits can be built up that fulfill the self−excitation conditions. According to this, we distinguish the RC oscillators by

- phase−shifting oscillators and
- Wien bridge oscillators.

Phase−shifting oscillators

The network which feeds back consists of a three or four−stage RC branch circuit which is also called "RC chain".

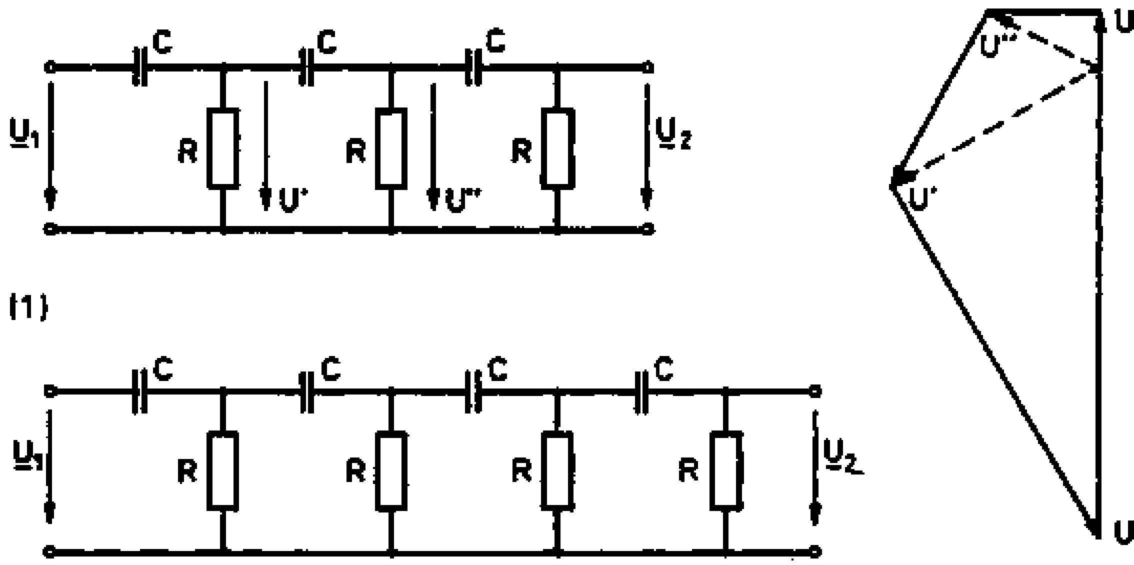


Figure 103 RC branch circuit (RC chain)

(1) three−stage,
(2) four−stage,
(3) vector diagram of voltages

The phase shift between the input voltage and the output voltage of a single RC element depends on the values of the components and on the frequency. The phase angle of ? = 90 deg. is not reached until f ? ? , but then the amplitude of the output voltage is zero. Actually, a single RC element can effect only a phase shift of ? < 90 deg.. In order to achieve the required phase shift of ? = 180 deg., therefore, at least three RC elements are needed. The vector diagram in Figure 103 illustrates how the phase shift is gradually effected by means of a three−element RC chain.

In connection with an emitter stage generating the required voltage gain, a simple RC oscillator can be built up.

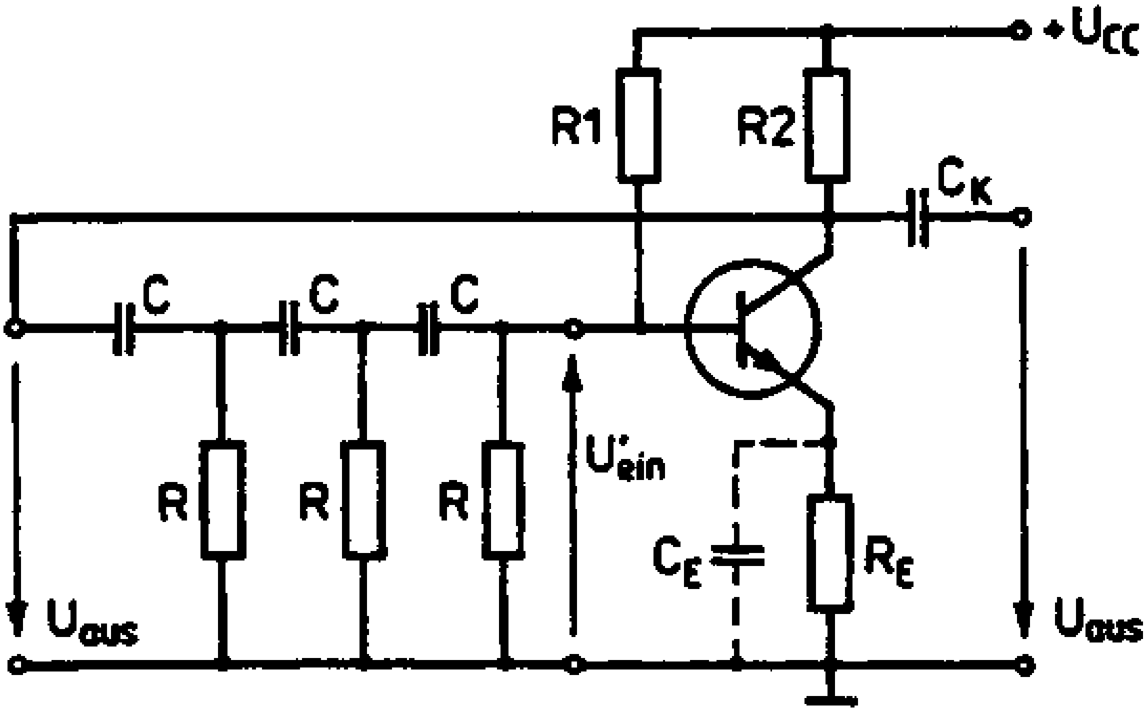


Figure 104 RC oscillator with phase−shift network

The input resistance of the amplifying stage must be high with respect to R. If not so, the RC chain is overloaded.

Another, possibility is to interchange R and C within the chain. This results in resonant frequencies which are two to six times higher.

Wien bridge oscillators

At a frequency of

$$f_r = \frac{1}{2 \quad RC}$$

The circuit shown in Figure 105 (1) (Wien circuit) features a phase shift equal to zero deg.

In connection with an amplifier circuit, which does not shift the phase and has a voltage gain of $v_u > 3$, oscillations can be excited. The amplifier circuit can be laid out e.g. as two−stage emitter circuit with negative feedback (in order to achieve $v_u = 3$). Hereinafter let us consider a circuit having an operational amplifier.

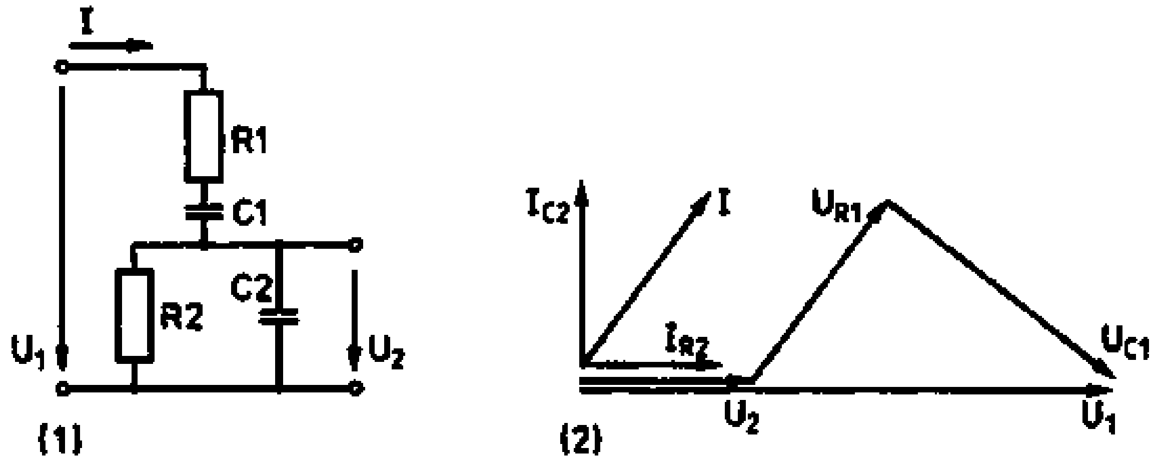


Figure 105 Explanation of the Wien bridge oscillator

(1) network,
(2) vector diagram

The circuit shown in Figure 106 is represented in (3) as closed−loop control. While through the Wien circuit a positive feedback is effected, R1 and R2 cause a negative feedback. The external components form a bridge circuit (2), to the diagonal branch of which the inputs of the operational amplifier are connected.

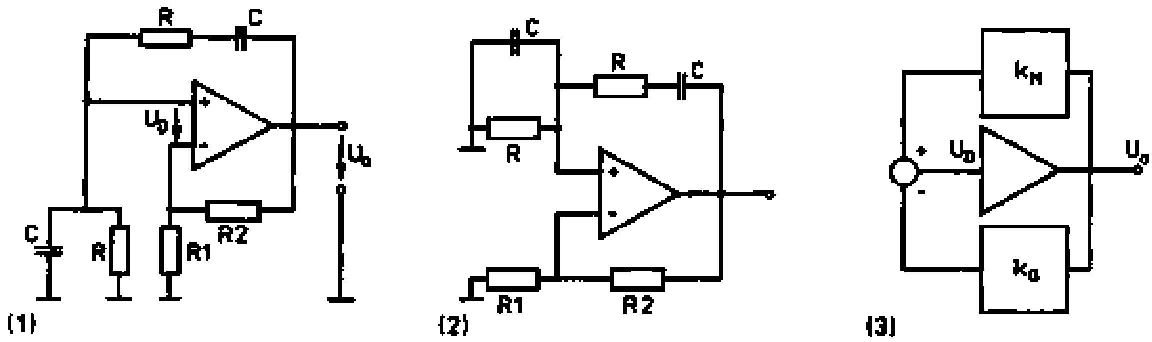


Figure 106 Wien bridge oscillator with operational amplifier

(1) basic circuit,
(2) representation of the bridge,
(3) representation as closed two−loop control

Through a suitable balance the positive feedback factor k_M is to be set at a slightly higher value than the negative feedback factor k_G.

So the oscillations can build up. If, in steady state,

$k_M = k_G$ (for v_b ? ?)

shall apply, the negative feedback branch must be provided with a resistor that is independent of the amplitude. For this purpose a field effect transistor can be used, which acts as voltage−dependent resistor below the pinch−off region. Figure 107 shows a schematic drawing. With the amplitude increasing, the resistance of the FET gets bigger and, consequently, also R' and the negative feedback ratio

$$k_G = \frac{R_1'}{R_1' + R_2}$$

The gain declines until kv = 1.

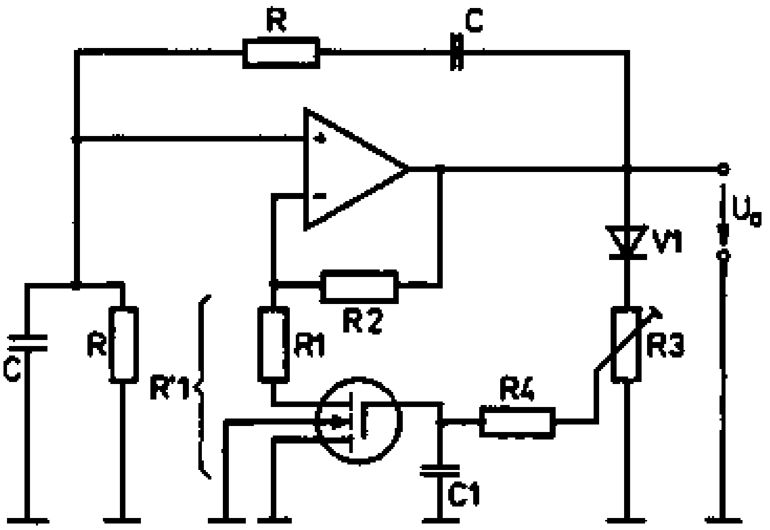


Figure 107 Amplitude limitation by a MOSFET in the negative feedback branch

1.4.7. Controllers

The functional unit "controller" serves to compare the values of an input with the value of an adjustable reference input and to emit an output signal depending on the result of such comparison and on the properties of the controller.

A comparison in the controller is subject to both quantities being available in the same physical state.

The properties of the controller as such are determined by its dynamic behaviour. In this connection, it is common practice to use also the step response for designating this behaviour. Accordingly, we distinguish

– proportional–action controllers (P controllers)
– integral–action controllers (I controllers)
– derivative–action controllers (D controllers)

Often, two or all three properties are interlinked.

These properties are obtained by feedbacks which, according to their dynamic behaviour, are classified as follows:

– rigid feedback (generating P action)
– derivative feedback (generating I action)
– elastic feedback (generating PI action)
– delayed feedback (generating PD action).

Each of the properties mentioned can be conferred upon an operational amplifier by selection of the proper feedback. Hereinafter, wired–up operational amplifiers are described as controllers.

P controllers

The inverting amplifier already known acts as P controller. It has the following proportional control factor:

$$K_P = \frac{\Delta U_a}{\Delta U_e} = v_{uD'} = -\frac{R_2}{R_1}$$

$$U_a = \frac{R_2}{R_1} \cdot \Delta U_e.$$

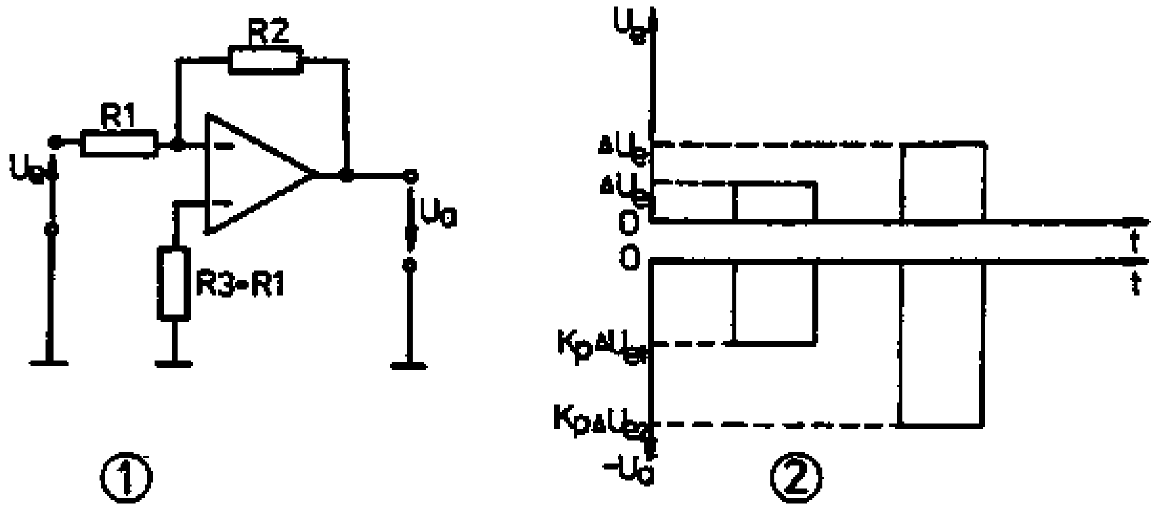


Figure 108 P controller

1 type of connection,
2 step response

By selecting suitable resistances R1 and R2 it is possible to change the value of the proportional control factor within broad limits. The resistance R3 is to reduce the effects of the offset i current.

The step response as per 108 (2) leads to the conclusion that the P controller emits, without delay, an output signal which is proportional to the variation at the input.

<u>I controllers</u>

When, in an inverting amplifier circuit, the resistor R2 in the negative feedback circuit is replaced by a capacitor, the operational amplifier acts as an integrator. The capacitor is charged by the output voltage. The output voltage increases until it is limited by the operational amplifier or until the input voltage disappears (in Figure 109 (2) indicated by broken lines).

According to the type of feedback, the rate of output voltage change depends on the amount of the input voltage. The capacitor C2 (Figure 109 (1)) transmits each variation of the output voltage onto the inverting input, thereby changing its charge state. When the charge equalization is reached, there is no negative feedback action any more.

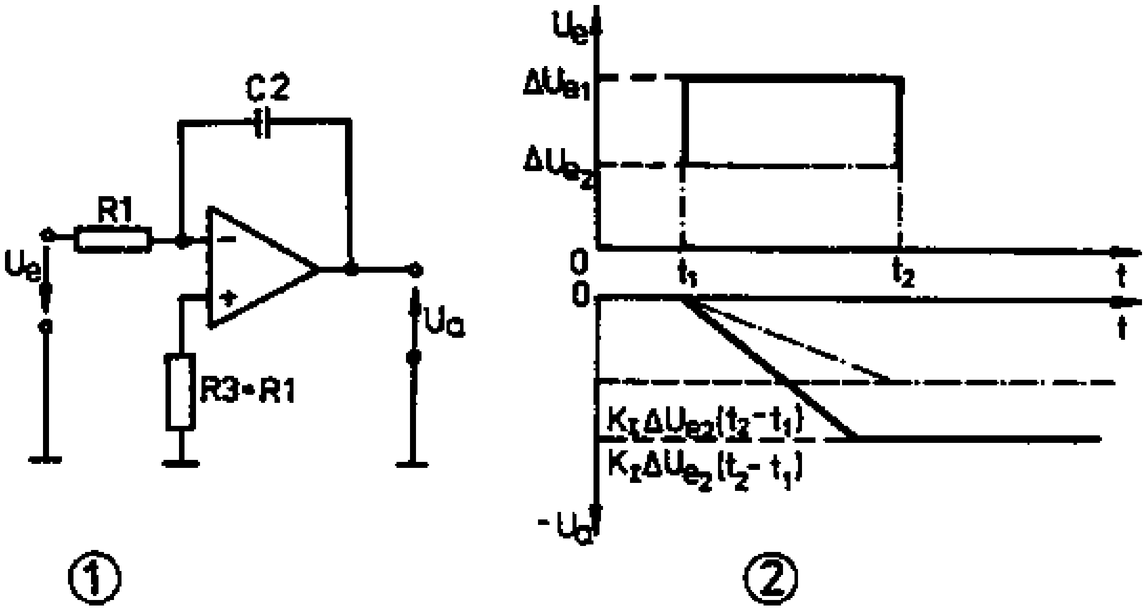


Figure 109 I controller

(1) type of connection,
(2) step response

The voltage through C2 depends on the amount of the input voltage. This is intimated by the course of the step response (109 (2)).

<u>D controllers</u>

Figure 110 shows a practical circuit for a D controller. This Circuit, however, acts derivative only for frequencies of

$$\omega << \frac{1}{R_2 \ C_1}$$

If the frequencies are higher, the controller develops a proportional action first and then an integral action.

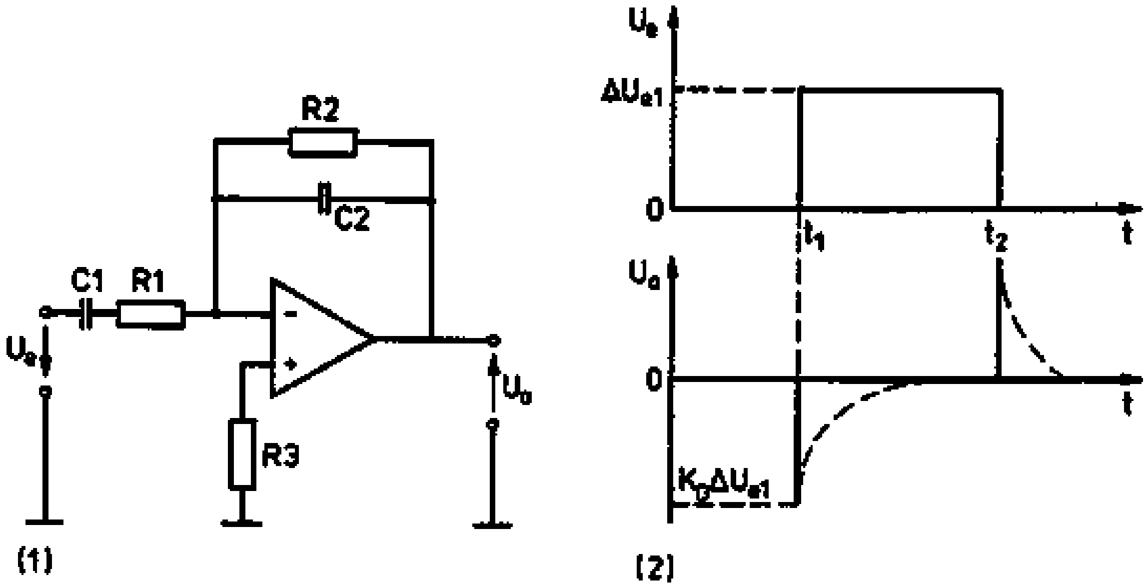


Figure 110 D controller

(1) type of connection,
(2) step response

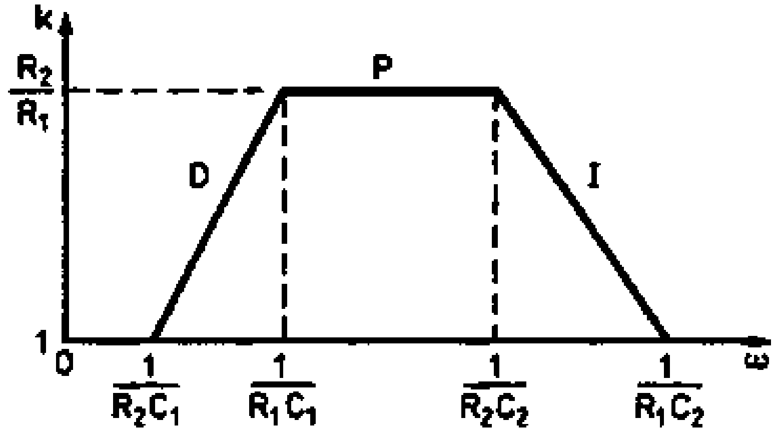


Figure 111 Frequency−dependence of the transient response of the modified D controller with an operational amplifier (idealized)

The frequency−dependence is illustrated in Figure 111.

In general, the following rule applies to a derivative action (Figure 110 (2)):

$$\Delta U_a \approx -R_2 C_1 \frac{d\,U_e}{1\,dt}.$$

The feedback circuit brings about the required derivative action in a limited frequency range only. As to sine−type input quantities this refers to the range for

$$\omega << \frac{1}{R_2 \quad C_1}$$

In such case, the following applies:

$$K_D = \frac{\hat{U}_a}{U_e} \approx -\omega R_2 C_1.$$

The output voltage depends on the rate of change of the input voltage. In the event of big voltage steps, the operational amplifier, therefore, is slightly overmodulated. Because of its limited frequency range and its tendency towards instability, a pure D controller is not used.

Since the action of a controller is always to be adapted to the controlled system, combined versions of the described basic types play an important part in engineering.

PI controllers

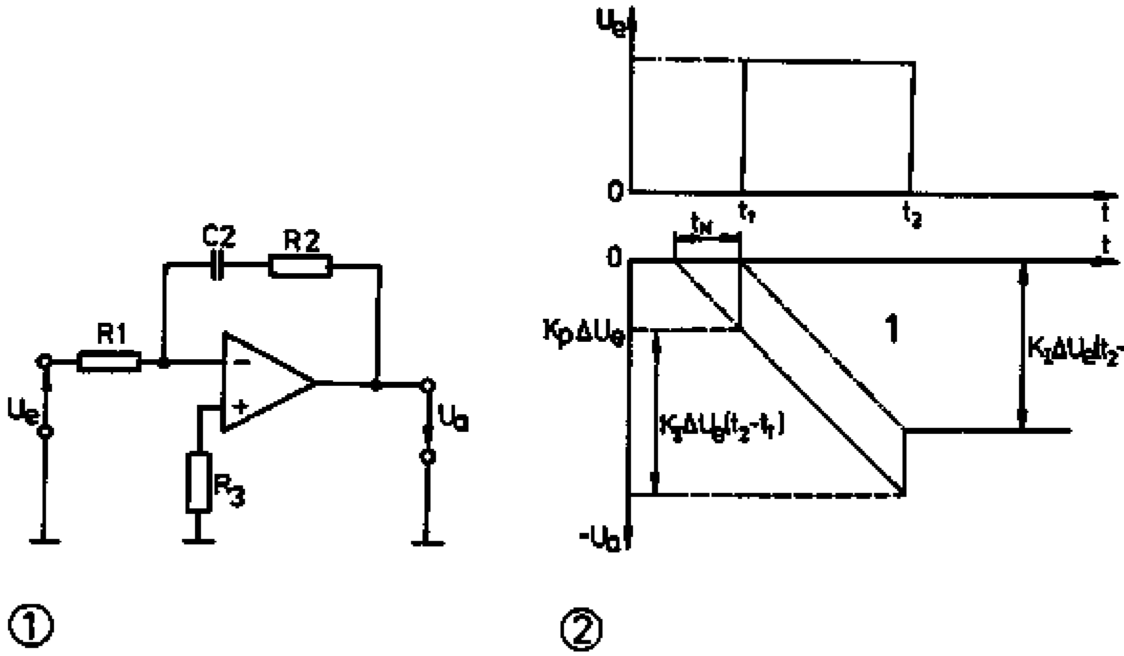


Figure 112 PI controller

(1) type of connection,
(2) step response, 1 integral action only

By combination of components in the feedback branch it is possible to superimpose the effects.

The integral−action time t_N is that thime which is required by the controller to achieve the same output value by pure I action as is immediately achieved by the P part. This means that a PI controller reacts more quickly than an I controller. The elastic feedback effect can bee seen in Figure 112 (2). For a moment, the controller reacts proportionally only, but then C2 is charged and the negative feedback effect becomes smaller and smaller. For t_N ? ? the I part is cut off. Then, the controller acts as pure P controller.

PID controllers

By combination of all three basic types a universally applicable but expensive and difficult−to−adjust type of controller is produced.

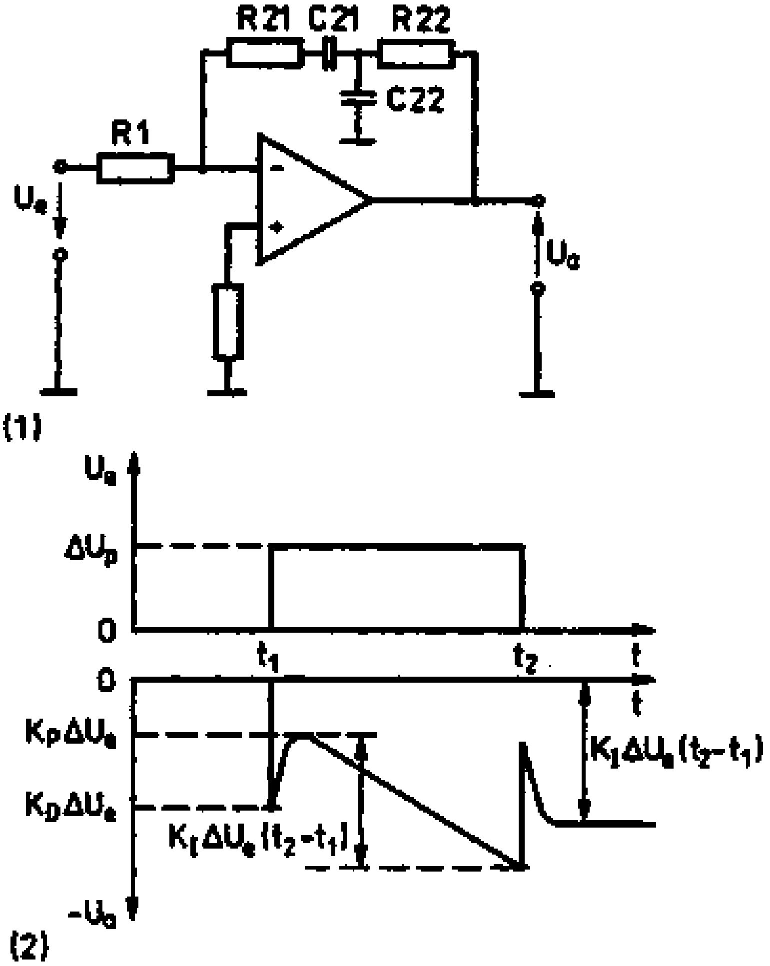


Figure 113 PID controller

(1) type of connection,
(2) step response

In general, the interrelationship between the input and the output value reads:

$$\Delta U_a \approx -K_P\left[\Delta U_e + K_I\ t_2 \Delta U_e dt + K_D \frac{d(\Delta U_e)}{dt}.\right]$$

Adaption to the control system is effected by setting the three values K_P, t_N and t_v on the controller.

The adjustment t ? ? or (and) t = 0 permits to reduce the PID action to a PD and a PI action, respectively, or a P action. The derivative time t signifies the immediate action of the controller upon a steady variation of the input.

It corresponds to that time which is required by a P controller to achieve that amount of the output which is adjusted by the D part at once.

This is shown in Figure 114 for the response of a PD controller to a linearly increasing input.

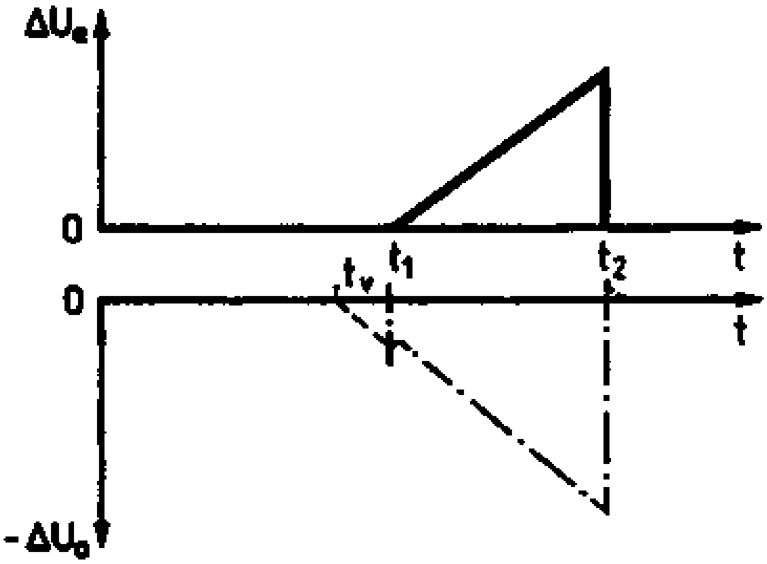


Figure 114 Definition of the derivative time t_V

The proportional control factor becomes rather intricate. It is, therefore, not mentioned herein.

Any other combined versions are of minor technological importance (PD) or without any sense (ID) because the feedback effects are contradicting each other.

All controller types mentioned herein have one fact in common: They are continuous controllers. Discontinuous controllers, which are also called switching controllers, are not considered herein.

1.4.8. Transformation and conversion

The functional unit "transformer" transforms an analogue input signal into another analogue input signal.

During this process standard signals are frequently emitted. Table 9 shows the international– standard signal ranges.

Table 9 Standard signal ranges

Signal carrier	Information parameters	Standard signal range
Direct current	Amplitude	0... 5 mA
		0...20 mA
		4...20 mA
		– 5...0...5 mA
Direct voltage	Amplitude	0...10 V
		–10...0...10 V

The standard ranges for various inputs permit standardization of the controllers (standard controllers).

The functional unit "converter" converts an analogue input signal into a digital output signal or vice versa.

Consequently, we distinguish

- analogue–to–digital converters (A.D.C.)
- digital–to–analogue converters (D.A.C.).

Since most of the measuring values appear in their analogue form and the servo units have to be triggered analoguously, but digital signal processing is of advantage both types are often employed.

In general, the term "transformer" is used as generic term.

Transformers

From the wide variety of transformers that can be used let us describe just a few here:

Pressure−to−amperage transformers (p/I transformers)

Such transformers permit to transform pneumatic or hydraulic control systems into electrical control systems. This is often important because in some workshops the use of electrical control systems is not admitted or admitted with certain restrictions only due to explosion hazards.

A Bourdon tube or a metal bellows generates a pressure−dependent deflection which is picked up by an inductive transducer and [fed to an amplifier. The amplifier supplies an output voltage which passes the load resistor R_L and a moving coil system. The moving coils generate a force which balances the original deflection (force balance). Consequently, the output amperage is proportional to the deflection, which, in turn, is proportional to the pressure.

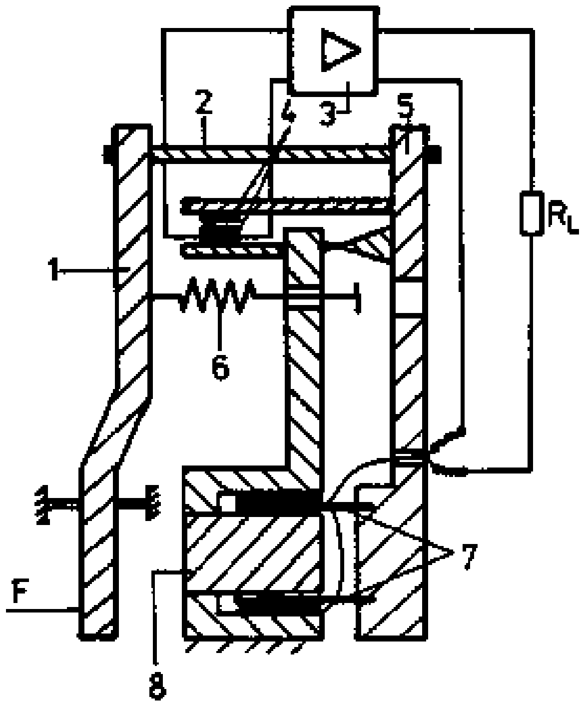


Figure 115 Schematic construction of a p/I transformer

1 force−path transformer
2 coupling rod
3 amplifier
4 inductive transducer
5 balance beam
6 zero setting device
7 moving coil
8 permanent magnet

In this connection, an operational amplifier featuring negative voltage and current feedback can be used.

Voltage−to−current transformers (U/I transformers)

An operational amplifier with negative feedback according to Figure 89 lends itself to voltage−to−current transformation.

Current−to−voltage transformers (I/U transformers)

Here, too, an operational amplifier with negative feedback can be used.

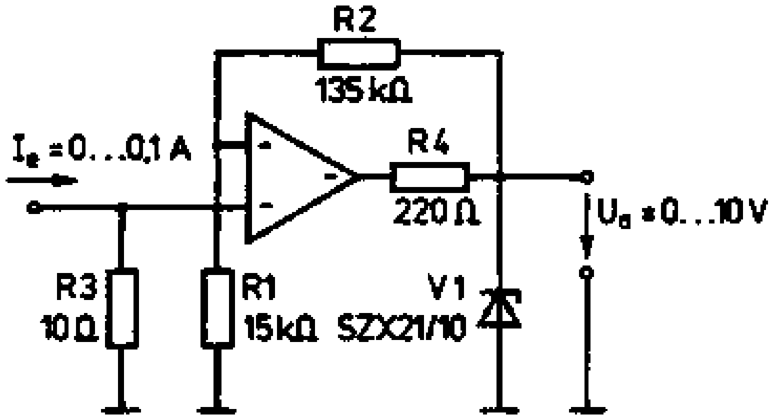


Figure 116 Basic structure of an I/U transformer for high input amperage

Figure 116 shows a schematic drawing of the transformation of a current of I_e = 0...100 mA into the standard voltage range of U = 0...+10 V.

The relatively high amperage of the input current would destroy the input transistors of the operational amplifier. For this reason, the input current is transformed into a voltage U_e = 0...1 V at the resistor R3, which is subsequently brought to the required output value by means of a voltage amplifier (U/U amplifier).

The following applies to the amplification.

$$V_{uD}\infty = 1 + \frac{R_2}{R_1} = 10.$$

The ratio of $\frac{R_2}{R_1}$ must be achieved by resistors, the values of which are in an E range. Since these values determine also the stability of the amplification, they must be high−resistive and feature close tolerances. The values selected here are R_2 = 135 k? and R_1 = 15 k? (tolerance ± 1%). The Z−diode V1 at the output limits the output voltage to 10 V. An offset compensation is recommended.

Voltage−to−voltage transformers (U/U transformers)

A voltage transformation is necessary in the event of transforming into a standard range or of a potential division. In the latter case, a voltage transformer is a must.

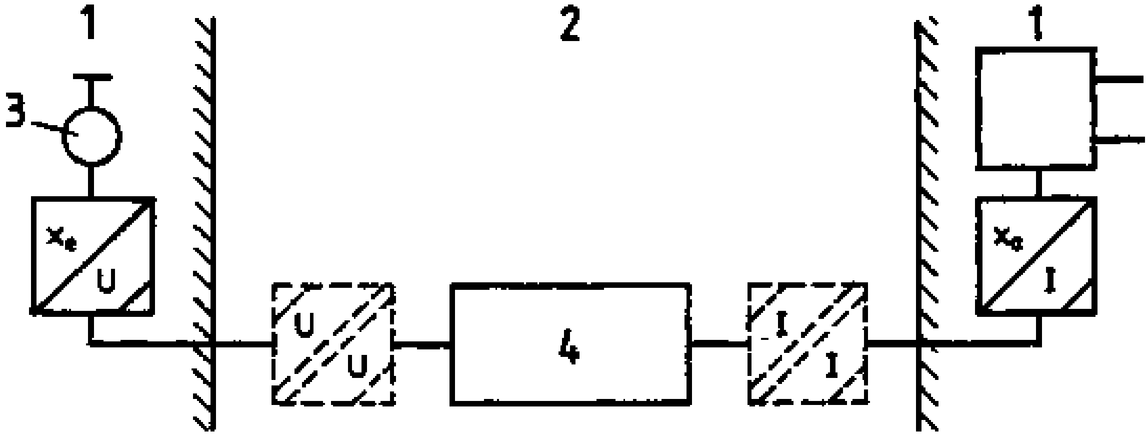


Figure 117 Use of potential dividers

1 area with explosion hazards,
2 area without explosion hazards,
3 sensor,
4 processing

In connection with electronic circuits, it is possible to combine the potential division with the transformation. The potential division is applied when connecting intrinsically safe I functional units with units which are not intrinsically safe. Intrinsically safe functional units can be installed in rooms with explosion hazards.

Intrinsic safety "i" is achieved when sparks or overtemperatures, which may arise, are not able to ignite an explosive gas–air mixture.

The circuit must be laid out so as to ensure that the sparks which may arise in the event of shorts or during switching operations, are of low energy or that the overtemperatures which may occur are negligible. In such event the required ignition energy is not developed.

Depending on the disturbance conditions (e.g. inadmissible modification of component parameters or damage) intrinsically safe circuits are classified into 3 categories (i_a, i_b, i_c).

As to areas where there is but a rare or temporary danger of explosion intrinsic safety can be ensured by a safety barrier, too. Figure 118 shows the circuit of a safety barrier. The z–diode V1 stabilizes the voltage at values of $U_z \lesssim < 6\ V$, R2 limits the amperage in the hazardous areas.

The Z–diode V2 provides additional safety; it is able to take over the functions of the diode V1 if this should fail. The fuse F1 protects the diodes against overload in the event of failure. The base of the Z–diode circuit must be connected to earth by a potential equalization line in the area with explosion hazards.

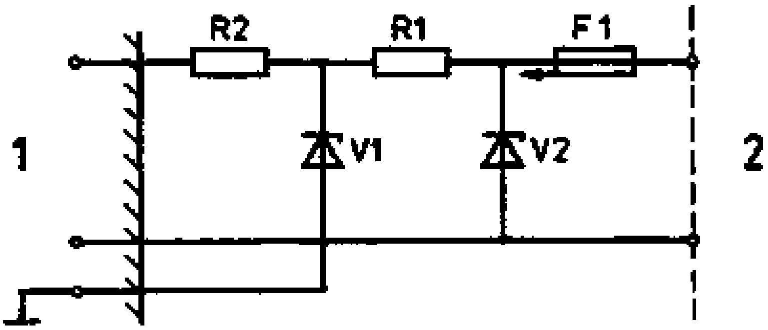


Figure 118 Circuit of a simple safety barrier

1 area with explosion hazards
2 unprotected area

<u>Converters</u>

The conversion of analoguous into digital signals and vice versa requires relatively intricate circuits. The expenditure increases, the higher the conversion accuracy required. In this book, just a few principles can be mentioned.

<u>Digital–to–analogue converters</u>

From the wide variety of possibilities we selected the current summation method. The summation is effected through the summation resistor R_S. Currents at a ratio of 1:2:4:8 are flowing through the graduated resistors in the emitter circuits when the respective transistors become conductive. Then, the dual figures 0 to 16 can be converted into an equivalent voltage at the resistor R_S. The accuracy depends on the tolerance of the resistors and the stability of the voltage U_{CC}.

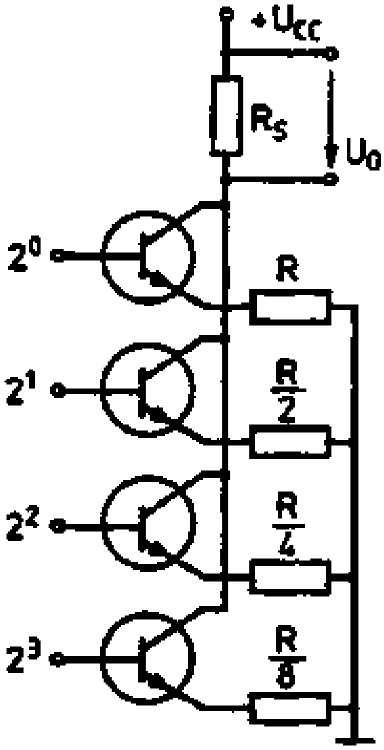


Figure 119 D/A converter for current summation

Analogue–to–digital converters

This conversion, too, can be made in various ways.

The process selected here is the time coding method. The value to be measured is converted into a direct voltage U_x. In the A–D converter a time–linear sawtooth voltage U_{Ref} is generated which is compared with U_x in a comparator. The comparator emits start and stop signals which control a gate. During the measuring time t_M this gate is open to the oscillations of the frequency "f". The frequencies are counted and displayed.

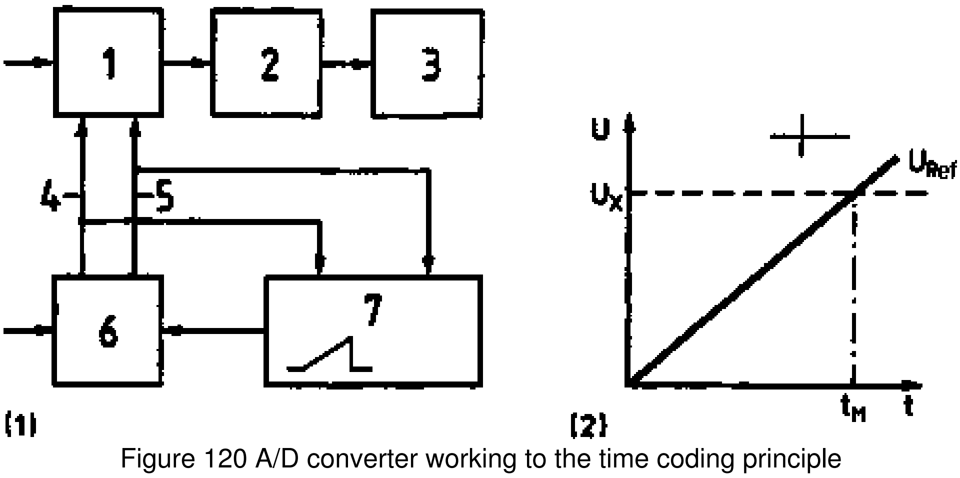


Figure 120 A/D converter working to the time coding principle

(1) general circuit layout,
(2) voltage behaviour
1 gate circuit,
2 counter,
3 display,
4 start,
5 stop,
6 comparator,
7 reference voltage

An up–to–date A–D conversion process is the dual slope method which is also called double integration process. The basic layout of the circuit and its working principle are represented in Figure 121. The input signal, the voltage U_M to be measured, is integrated through the constant time t ? 20 ms. Once this time is over, the integration input is switched to a reference voltage U_{Ref} which is opposite in polarity with respect to U_M. This causes the charge of the integration capacitor C to decay again. At the zero passage of the capacitor voltage t_3 (Figure 121 (2)) this process is interrupted by the control unit. In each stage of integration the counter counts the pulses fed by the timing pulse generator. Charge losses at the integration capacitor being excluded, the measuring result exclusively depends on the stability of the reference voltage.

With the quantities

Z_1 count after passing of $?t_1 = t_1 - t_0$

Z_2 count after passing of $?t_2 = t_3 - t_2$

$\frac{Z_1}{Z_2}$ becomes $\frac{U_M}{U_R}$.

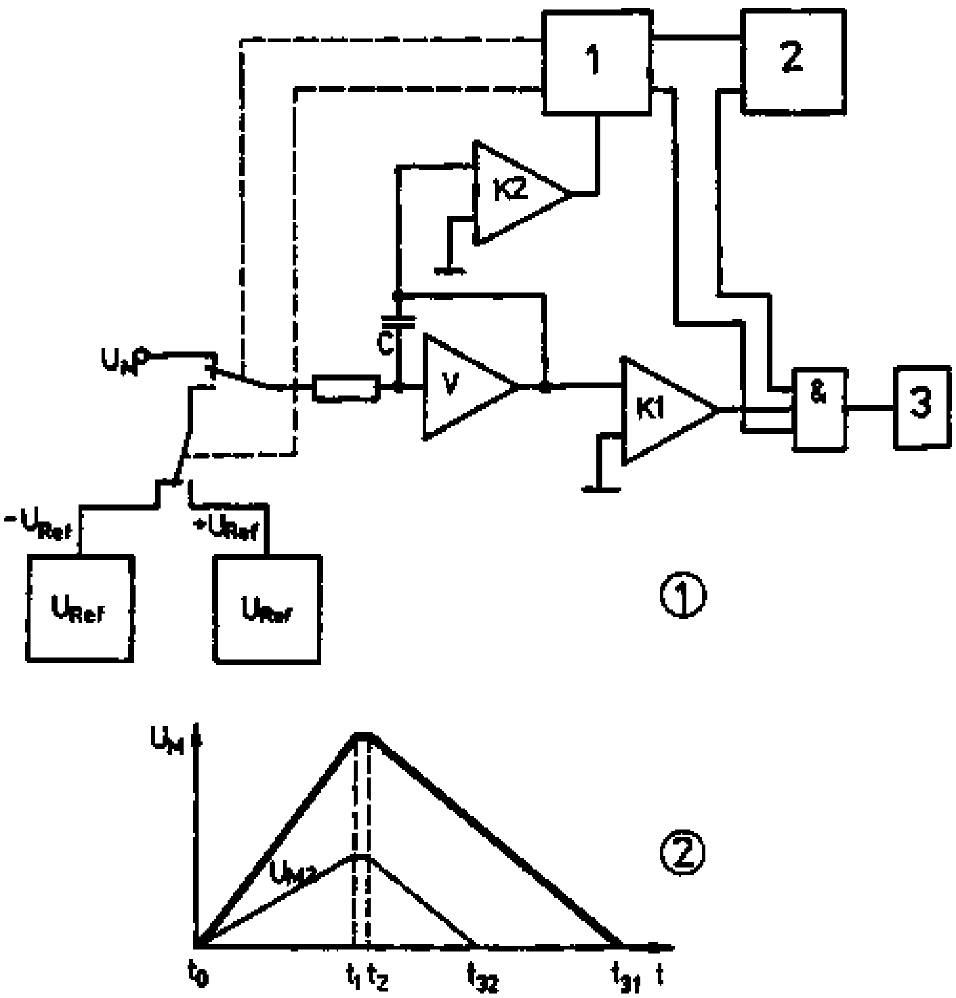


Figure 121 A/D converter working to the dual slope method

(1) general circuit layout,
(2) voltage behaviour
1 control unit,
2 clock cycle,
3 counter

The first integration time, which is also called signal integration time, was selected with about 20 milliseconds, in order to suppress interferences which are coupled with the mains frequency.

An analogue−to−digital conversion to this method is effected by a circuit, too. It can convert voltages in the range between − 99 ... + 999 mV. A general wiring diagram is represented in Figure 122. This diagram illustrates the circuit part developed by the circuit manufacturers as well as the advantages of integrated circuits.

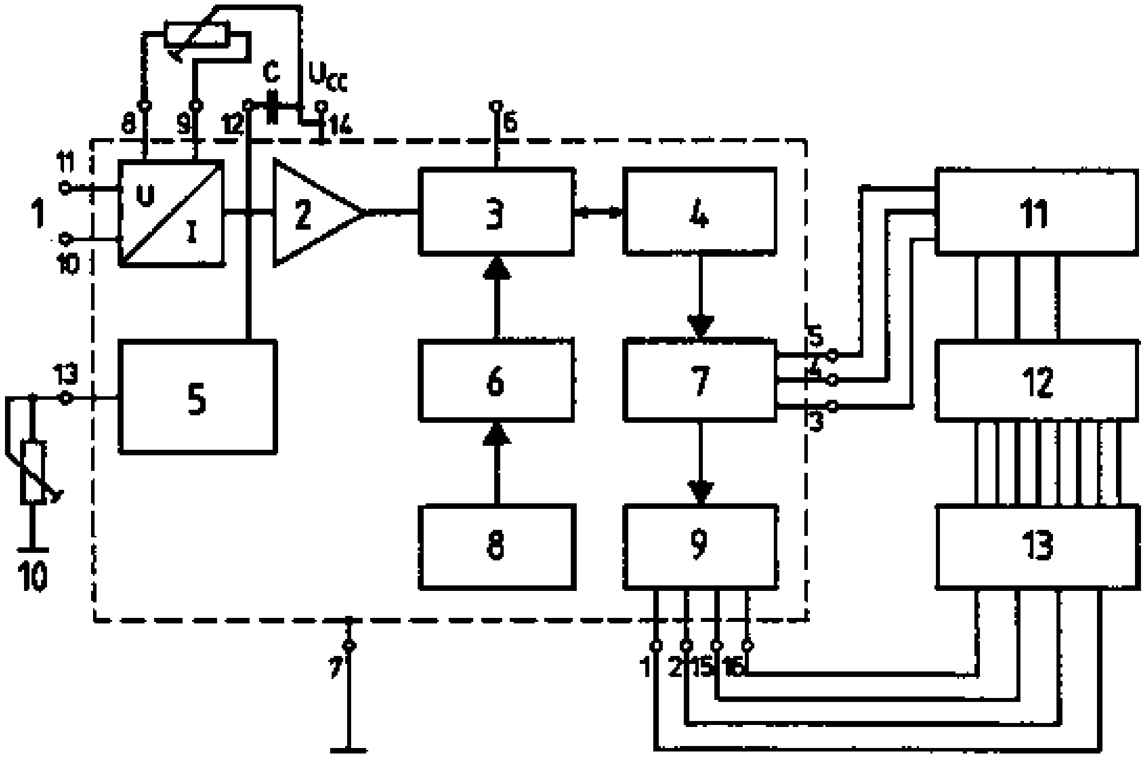


Figure 122 A/D converter with an integrated circuit

1 input,
2 comparator,
3 control logic,
4 counter,
5 reference voltage source,
6 divider,
7 multiplexer,
8 oscillator,
9 matching circuit,
10 final–value adjustment,
11 demultiplexer,
12 display,
13 decoder

1.5. Digital circuits

1.5.1. Definitions and requirements

Special circuits are used to process digital signals. These circuits make use of the feature of such signals to be able to accept discrete states only. The employed electronics components can function as switches for the binary signals frequently used. In this function, the transient response of the components and the circuits built up with them is important only at the two possible points, on state and off state. The transition from one state to the other one is to be effected as fast as possible. This requires considerations different from those of analogue technology. This technology has developed a special language and the relatively independent field of digital technology, Since they have an immense technical importance, only circuits for the processing of binary signals shall be described herein. Binary signals have only two states which are identified as 1 or 0. These states are also called logic states, because a special propositional logic has been developed with them. Each state is usually called bit (binary digit). So each bit can have the meaning 0 or 1. By a respective assignment, one bit can transmit two data, as e.g. condition met ≙ ; condition not met ≙ 0. If more than two data have to be transmitted, several bits are combined to a data word. A definite coding is set up for such a data word, which is also called byte and mostly consists of 8 bits. The frequently used dual code relates a power of 2 to the position of the bit:

1st position: 2^{0}
2nd position: 2^{1}
3rd position: 2^{2} etc.

Table 10 shows how the numbers from 0 to 15 can be digitized with 4 bits.

The data words of 4 bits length are usually called tetrad. In general, 2^{n} different data can be transmitted with n positions. $m = 2^{n}$

m – set of data
n – number of positions of the data word

Thus, a data word (byte) consisting of 8 bits (byte) can transmit $m = 2^{8} = 256$ data.

The bits of a data word can be transmitted all at the same time, that means by parallel transmission, using one line for each position or one by one, i.e. by serial transmission, using only one line for all positions. Parallel transmission is very fast and is often used in microprocessors. The group of lines used is then referred to as bus.

If the states 0 and 1 are to be transmitted, an adequate electric signal is assigned to them. Usually, such a signal corresponding to a voltage range, of which the more positive voltage is assigned to the signal level H (high) and the more negative voltage to the signal level L (low).

Table 10 Example for the conversion of a decimal code into a binary code

Decimal number	**Binary number**			
	4th position (2^3)	**3rd position (2^2)**	**2nd position (2^1)**	**1st position (2^0)**
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

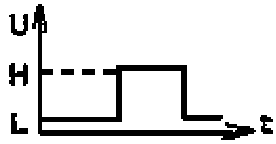
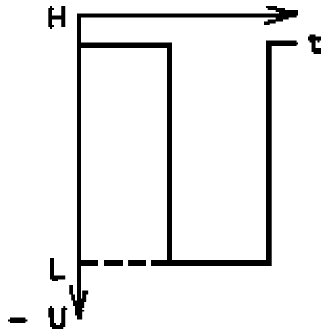
Designation	Correspondence	Voltage level
Positive logic	H ≙ 1 L ≙ 0	
Negative logic	H ≙ 0 L ≙ 1	

Table 11 Representation of positive and negative logics

The assignment of the logic states to the signal levels is optional. Usually, the higher voltage is allocated to the logic state 1. This allows the possibilities shown in table 11. TTL circuits, for example, work on the basis of positive logic, p−MOS circuits on the basis of negative logic.

Digital signals can be interconnected with each other as well as analogue signals can. This is done in accordance with logic propositions which can be simple or more complex. Such interconnections are widely used in the field of automation engineering* For example: a machine is to be switched on and off or operated from place 1 or place 2; an autoclave is to be heated only when it has been filled and its cover has been closed; starting of a driving motor shall only be possible if the load is declutched and the starter is in the off position and the temperature of the motor has not exceeded a limit.

Interconnections like these examples are combinations of conditions. Digital circuits that perform such combinations are called combinatory circuits. Another kind of interconnections is built up, for instance, if a fixed sequence of actions has to be observed when a plant is started up. So action 2 must not be possible until action 1 has been finished. For this purpose, the performance of actions has to be stored. Digital circuits allowing such interconnections are referred to as sequential circuits.

1.5.2. Combinatory circuits

Combinatory circuits are able to logically interconnect several input quantities (input variables).

The basic logical operations are:

NOT (negation)
AND (conjunction)
OR (disjunction).
Very often, the negation is combined with other operations:
NOT AND − NAND
NOT OR − NOR

NOT Interconnection

A NOT interconnection (negation) is only possible by means of an active component, usually a transistor. The logical operation NOT requires:

An output signal y is only possible in NOT interconnections if there is no input signal x.

In short this is expressed as follows: $y = \overline{x}$

(read: y equal x not or x cross).

Such propositions have an immense practical significance. Starting a plant, for example, must only be possible if certain limits have <u>not</u> been exceeded.

A negation can simply be performed by means of a relay with a rest contact. The logical assignments are clearly shown in a truth table (state table; functional diagram; table of values).

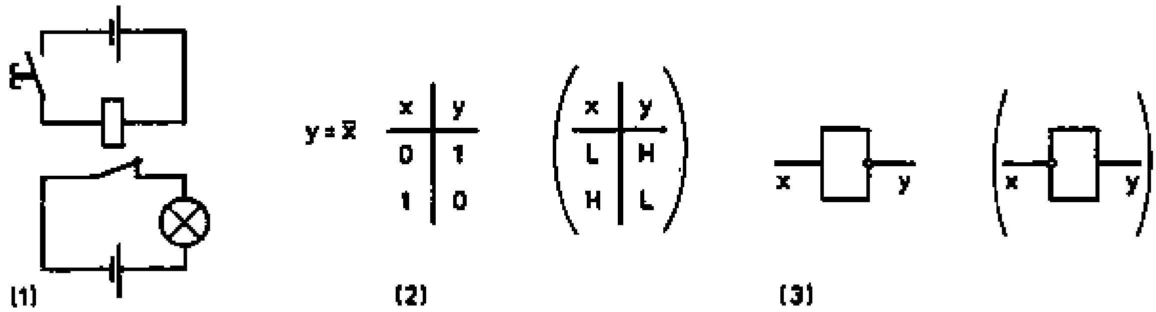


Figure 123 Negation by means of a relay

(1) type of connection,
(2) truth table,
(3) circuit symbols for a negator

If the negation is to be performed by a transistor circuit, the transistor's bias point must have two stable states: switch closed – high current intensity; switch open – current intensity nearly zero. Here, too, bias points can only lie on the resistance line, like in analogue technology.

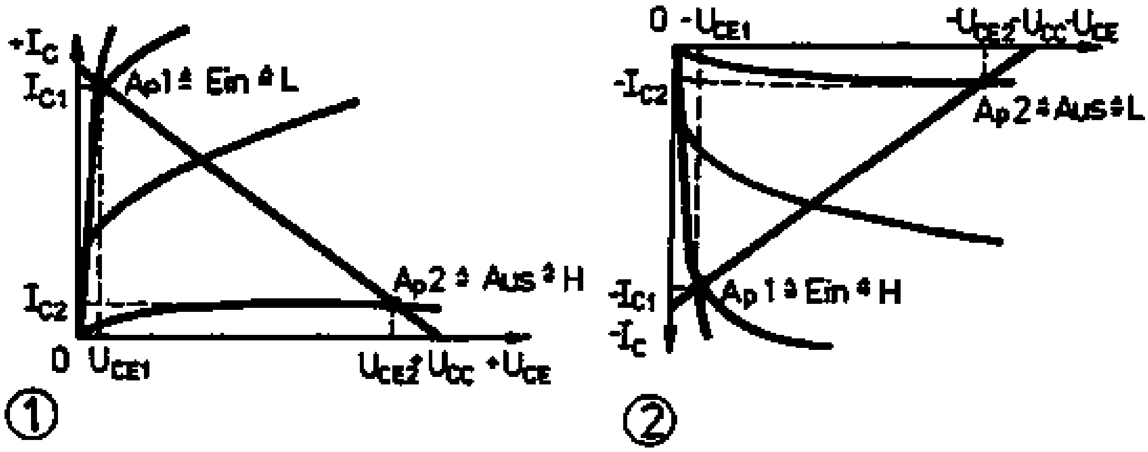


Figure 124 Bias points for a transistor operated as switch

(1) positive logic,
(2) negative logic

The required circuit has to be designed in such a way that both final positions of the bias point are definitely reached. That means:

– In the "on" position the base current I_{B1}. has to become so intense that U_{CE1} decreases as much as possible ($U_{CE1} = U_{CEsat}$). For that purpose, the transistor is over–modulated, the base current intensity is chosen m times higher than it would be necessary for $I_{C1} = h_{21E} I_{B1}$. Instead of I_{B1} the base current $I_{Bü}$ flows.

– In the "off" position the relation shall be U_{CE2} ? U_{CC}. For that purpose the transistor has to be blocked, what actually is achieved with $I_B = 0$. For reasons of safety usually an off–state voltage U_{BB} is applied, that biases the base–emitter junction in blocking direction.

When calculating the circuit elements, the voltage level, which corresponds to the level H or L, has to be known. Usually, lower or upper limits are given.

Figure 125 shows a circuit for a negation using MOSFET. Negator circuits are also referred to as inverters. Transistor V1 acts as load resistance, transistor V2 as amplifier. As long as the input voltage is lower than the threshold voltage U_{TO}, V2 is blocked and the output voltage amounts to $U_{DD} - (U_{TO})_{V1}$.

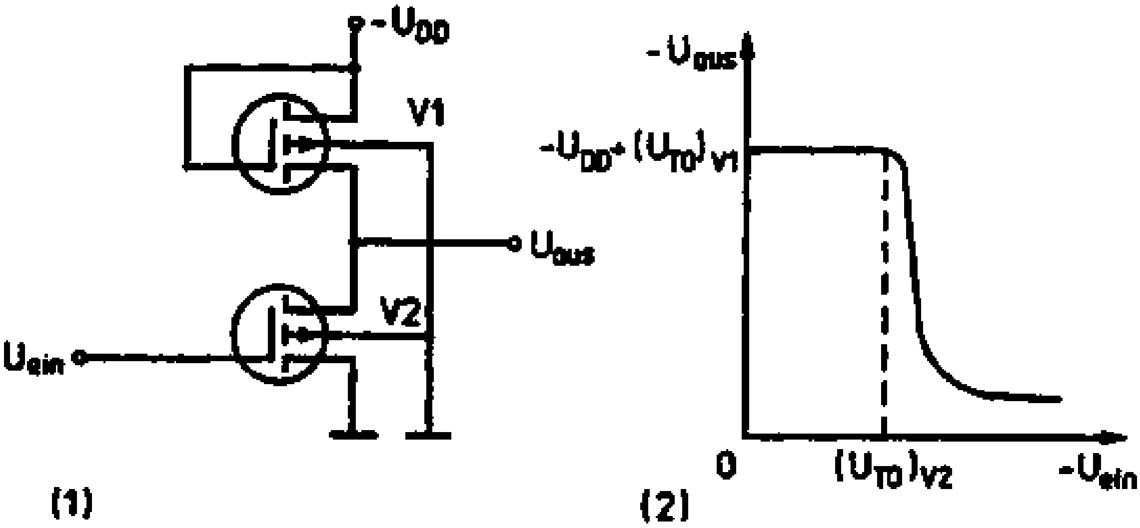


Figure 125 MOSFET inverter

(1) type of connection,
(2) transmission characteristic

The circuit for p−channel MOSFET (enhancement type) shown in Figure 125 can also be built up with other MOSFET types. Highly interesting solutions result from a simultaneous application of p−channel and n−channel MOSFET. This kind of applications is called complementary MOS or, in short, CMOS or COSMOS. In the CMOS inverter basic circuit shown in Figure 126, one transistor is always blocked. The result is a very low power input. Modulation requires a voltage $(U_{TO})_{T1} < U_{in} < (U_{TO})_{V2}$. If the output voltage is to have positive and negative values, too, a second operating voltage + U_{SS} is required.

MOS inverters are the basic circuit of digital MOS circuits.

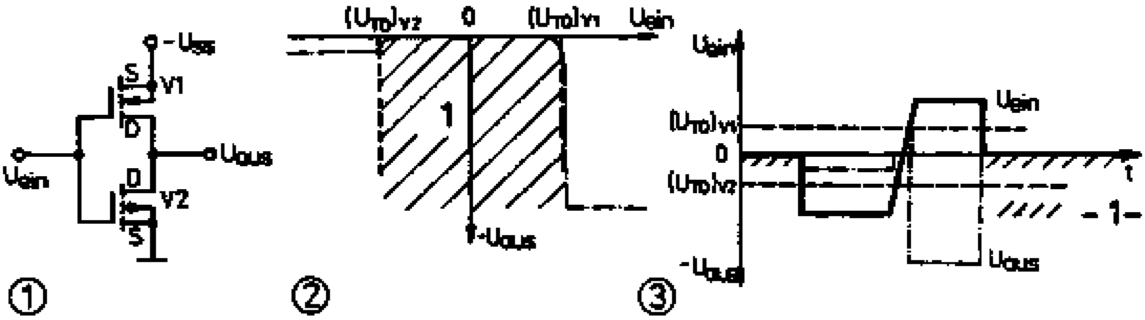


Figure 126 CMOS inverter

(1) basic circuit,
(2) transmission characteristic,
(3) time behaviour $U_{out} = f\ (U_{in})$

AND Interconnection

An AND interconnection, also called conjunction, describes the following logical operation:

An output signal y occurs in AND interconnections if there are two or more input signals at the same time.

For three input signals this means in short: $y = x_1x_2x_3 = x_1 \wedge x_2 \wedge x_3 = x_1\ \&\ x_2\ \&\ x_3$.

A typical conjunction is, for instance, if the first prize in a game is subject to the condition that 18 points are made with one cast and 3 dice, that means with die no. 1 and die no. 2 and die no. 3 six points each.

In a relay circuit a conjunction is performed by series connection of make−contact elements.

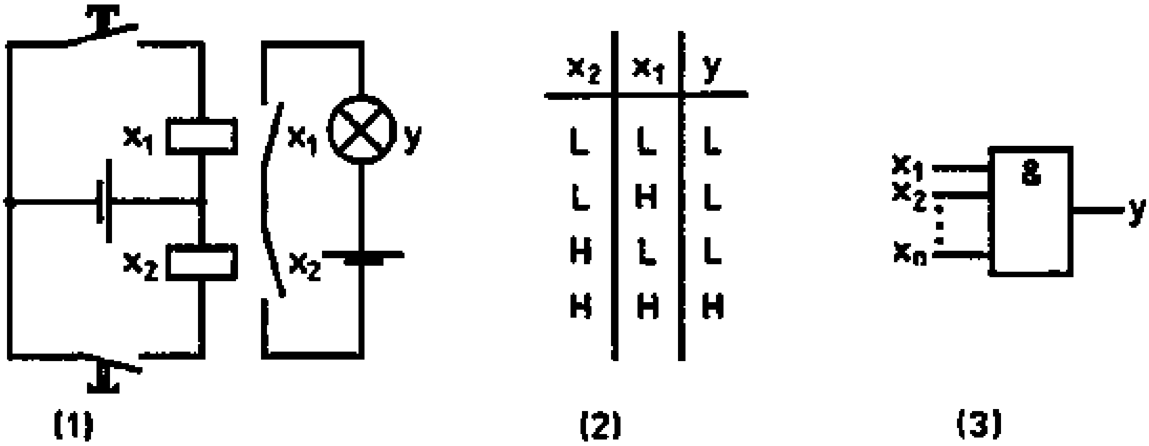


Figure 127 Conjunction by means of a relay

(1) type of connection
(2) truth table, L contact open, lamp is dark, H contact closed, lamp lights up,
(3) circuit symbol

A diode circuit as shown in Figure 128 avoids the disadvantages of a relay circuit, such as long switching times, low reliability and chattering of contacts. At the output y voltage does only occur if all inputs x_1 ... x_n are laid on the H level. To both circuits applies: $y = x_1 \wedge x_2 \wedge x_3 \ldots \wedge x_n = x_1 x_2 x_3 \ldots x_n$.

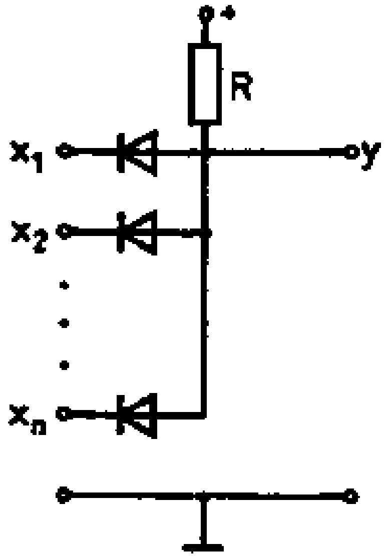


Figure 128 Conjunction by means of diodes

The L level corresponds to the flow voltage of the diodes, in; case of Si diodes U_F ? 0.7 V. The H level depends on the load of the output, without load applies $H \hat{=} +U$. Since there must be a clear difference between H level and L level, the load capacity of this ADN element is limited. Since the H level and the L level are given, the truth tables apply to positive as well as to negative logic. The logic states are assigned to the levels.

The logic families are given their names according to the type of the employed components which determine the level limits for H and L. So, the circuits shown (Figures 127 and 128) belong to

– Relay Logic (RELOG)
– Resistor−Diode Logic (RDL).

<u>OR Interconnection</u>

An OR interconnection or disjunction describes the following logical operation:

An output signal y occurs in OR interconnections if there is at least one out of two or more input signals.

For three input signals this means in short $y = x_1\ x_2\ x_3 - x_1 + x_2 + x_3$.

Figure 129 shows possible technical versions. If in the circuit of Figure 129/2 only one diode is asserted to the H level (positive logic), this level occurs at the output as well, and all the other diodes block.

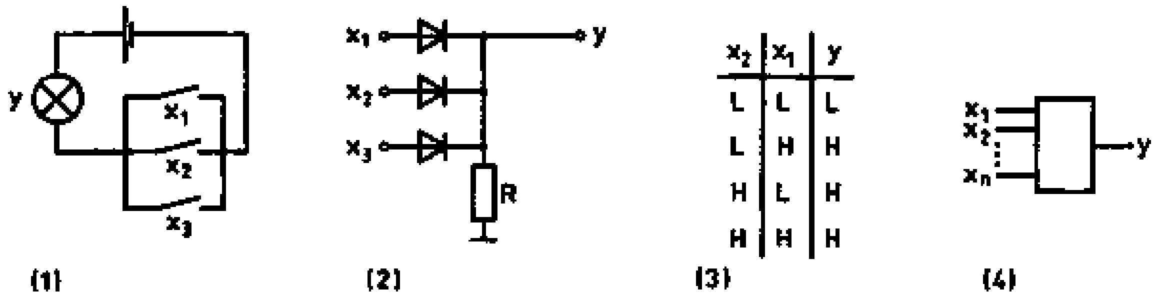


Figure 129 Disjunction

(1) relay logic,
(2) resistor−diode logic,
(3) truth table for two input variables,
(4) circuit symbol

The disadvantage of diodes that a negation cannot be produced is eliminated if diodes or resistors are coupled with transistors. The results of such couplings are the logic families

− Resistor−Transistor Logic (RTL)
− Diode−Transistor Logic (DTL).

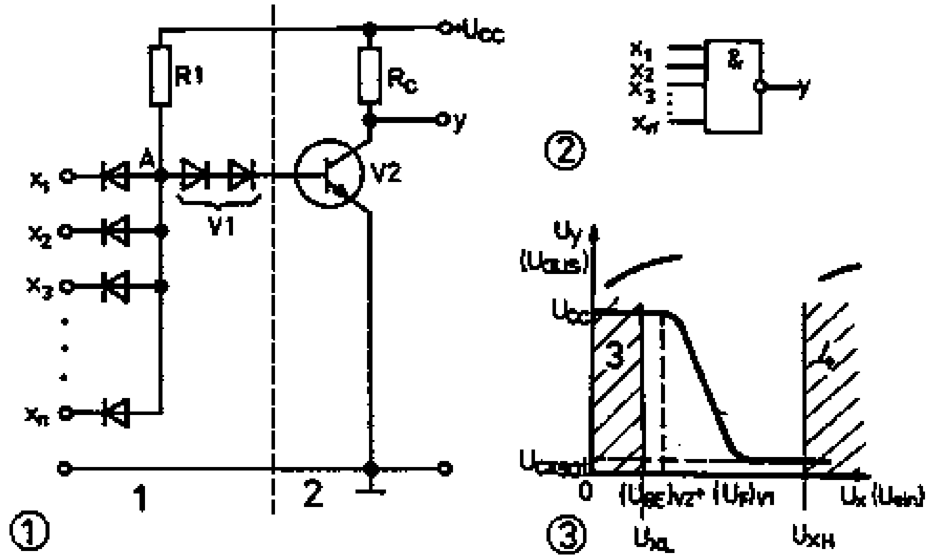
<u>NAND and NOR Interconnections</u>

If an AND element is combined with a negator, the result is a NOT − AND interconnection. This denomination is usually shortened to NAND.

Similar to that, a NOT − OR interconnection consisting of an OR element and a negator is called NOR.

<u>NAND Interconnection</u>

Figure 130 shows a circuit performing a NAND interconnection. It is combined of a diode AND element and a negator. The diodes V1 are employed to support the blocking of the transistor V2. A set maximum input voltage $(U_{inmax})_L = U_{xL}$ for the L level and a set minimum input voltage $(U_{in\ min})_H = U_{xH}$ for the H level guarantee definite output levels. The ratio of these limit values to the voltage levels that switch over the NAND element, is the static interference ratio.



x_3	x_2	x_1	y
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

④

Figure 130 NAND element

(1) diode−transistor logic circuit,
(2) circuit symbol,
(3) transmission characteristic,
(4) truth table for three input variables
1 AND element, 2 NOT element, 3 L level, 4 H level

The output voltage is $U_y = U_{CC}$ = H level, if one of the inputs x_1 ... x_n is asserted to the L level. In this case, the flow voltage of a diode lies between point A and earth (Fig. 130(1)). It is not sufficient to open diode V1 and to fully modulate transistor V2. The transistor is blocked, and an operating voltage occurs at its output if the load can be neglected. The output's permissible load is given with the load factor N_a. This load factor, also described as fan−out, amounts to the multiple unit load current.

If all inputs lie on the H level, the transistor V2 is modulated to saturation via R1 and V1, and its saturation voltage U_{CEsat} occurs as output voltage. It lies in the range of the L level. The truth table shown in Figure 130 (4) describes the general context.

$y = x_1 \wedge x_2 \wedge ... \wedge x_n = x_1 x_2 ... x_n$

(read: y equal x_1 and x_2 and ... x_n not)

It is obvious that an input L level immediately switches the output to the H level.

At the input of NAND elements the L level dominates.

A typical field of application of a NAND element is the gate circuit.

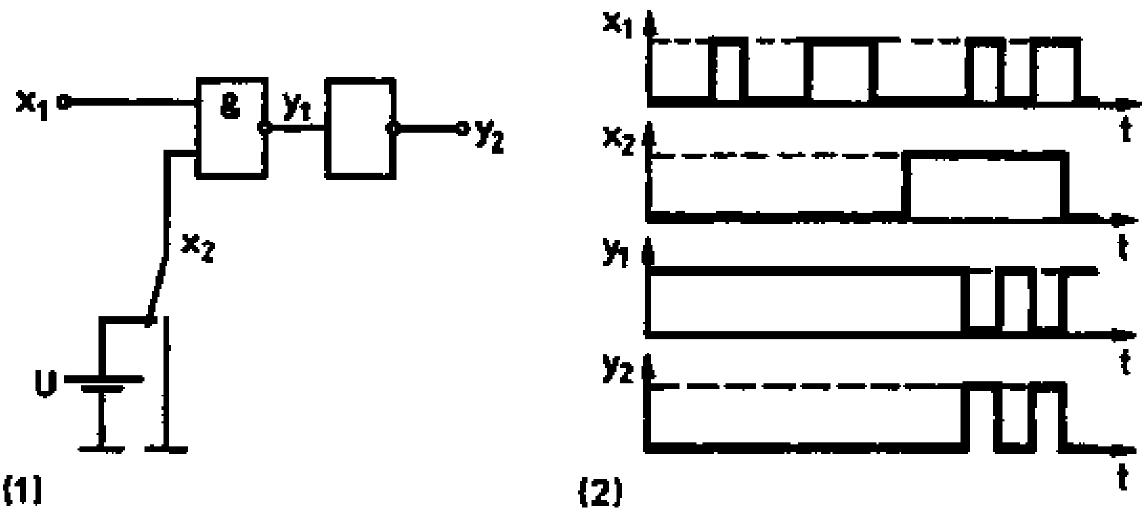


Figure 131 Use of a NAND element as gate circuit

(1) type of connection (symbolized),
(2) pulse diagram

The original pulse polarity is restored by an additional negator. If the diode V1 of the NAND element (Figure 130 (1)) is eliminated, the transistor V2 and the diodes serving for the AND interconnection can be combined and replaced by a transistor with several emitters (multi−emitter transistor).

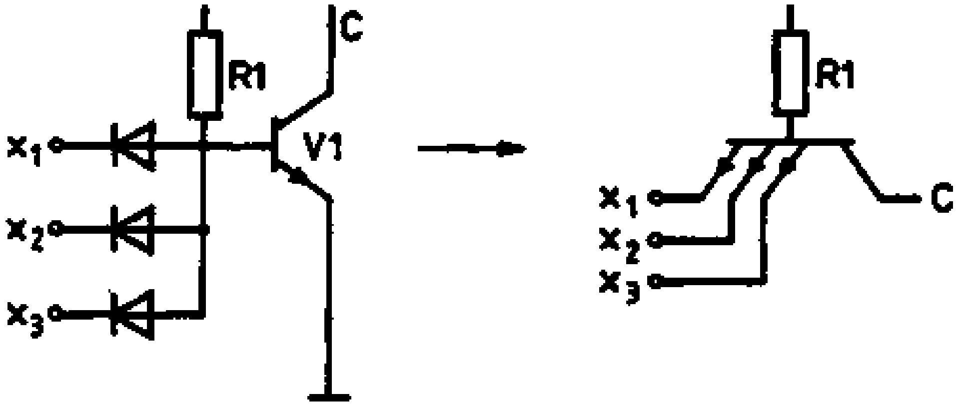


Figure 132 Transition to a multi−emitter transistor

This multi−emitter transistor is the core of a new logic family, the transistor−transistor logic (TTL), which at present is the most important one of all logic families. Integrated circuits contain, above all, transistors, since they require the same production costs but less space than diodes. Using MOSFET, that can well be used as resistors, transistors are integrated, exclusively.

The basic element of the TTL standard series 74 is the NAND interconnection. The simpliest form is the NAND interconnection of two inputs. It is referred to as dual NAND or dual NAND gate. The circuit is shown in Figure 133.

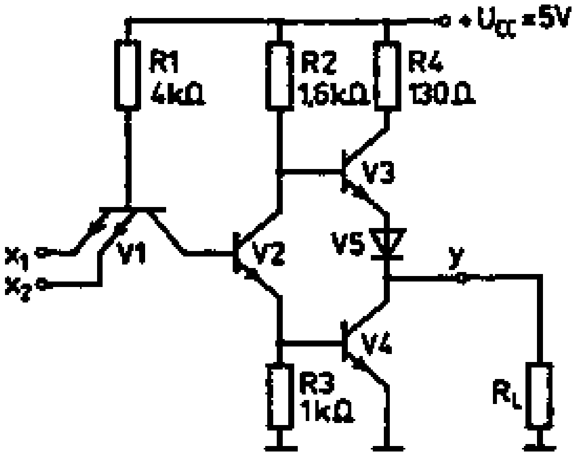


Figure 133 Internal circuit of a dual NAND gate of the TTL series

If both or one of the inputs are connected to earth (L level), the base current of transistor V1 flows to earth, and V2 remains blocked. Then V3 receives a base current over R2 and connects through. A voltage (H level) occurs at the output y.

If both inputs are connected by $+U_{CC}$, the base current flows from V1 to the collector. The pole−zero transition base −collector is no longer blocked, since the base potential is more positive than the collector potential. Thus transistor V2 is connected through, and a voltage occurs at R3 that connects through V4. Earth potential (L level) occurs at the output y. Now transistor V3 cannot connect through since its base potential is too low. This is supported by diode V5, the flow voltage of which is added to the base−emitter voltage of V3. With the input connection as described here, the potential at collector V2 amounts to about 0.9 V. The gate output voltage of U_L ? 0.2 V and the lacking diode V5 result in U_{BEV3} ? 0.7 V and thus the opening of transistor V3. However, this is not wanted with an H level at the gate input. Together with diode V5 the collector potential of V2 must amount at least to 1.6 V to open V3. This value is not achieved, and so V3 remains−blocked.

In the moment of switching both transistors V3 and V4 are conductive for some microseconds. During this short time a heavy pulse−shaped current flows that is produced by so−called supporting capacitors in the circuits. Producers demand ceramic disk−type capacitors of C = 10 nF to be connected to each circuit directly between operating voltage and earth. If such supporting capacitors are not applied, the peak current produces voltage drops and thus faulty switching of the gates.

The type of output stage circuit chosen in this series does not allow a parallel connection of outputs. In the case of one H−level output and one L−level output the operating voltage is shorted. The flowing short−circuit current of about 50 mA destroys at least one circuit. However, a parallel connection of the outputs is possible if gates with open collector output are used. Thus an additional OR interconnection can be produced, that is referred to as WIRED ON.

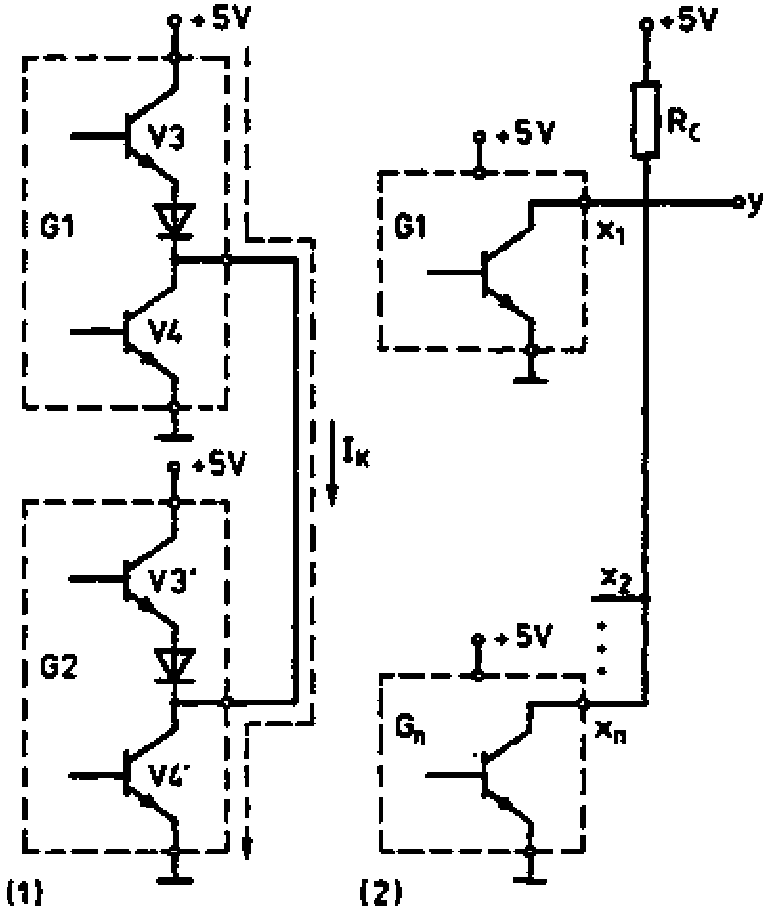


Figure 134 Parallel connection of circuit outputs

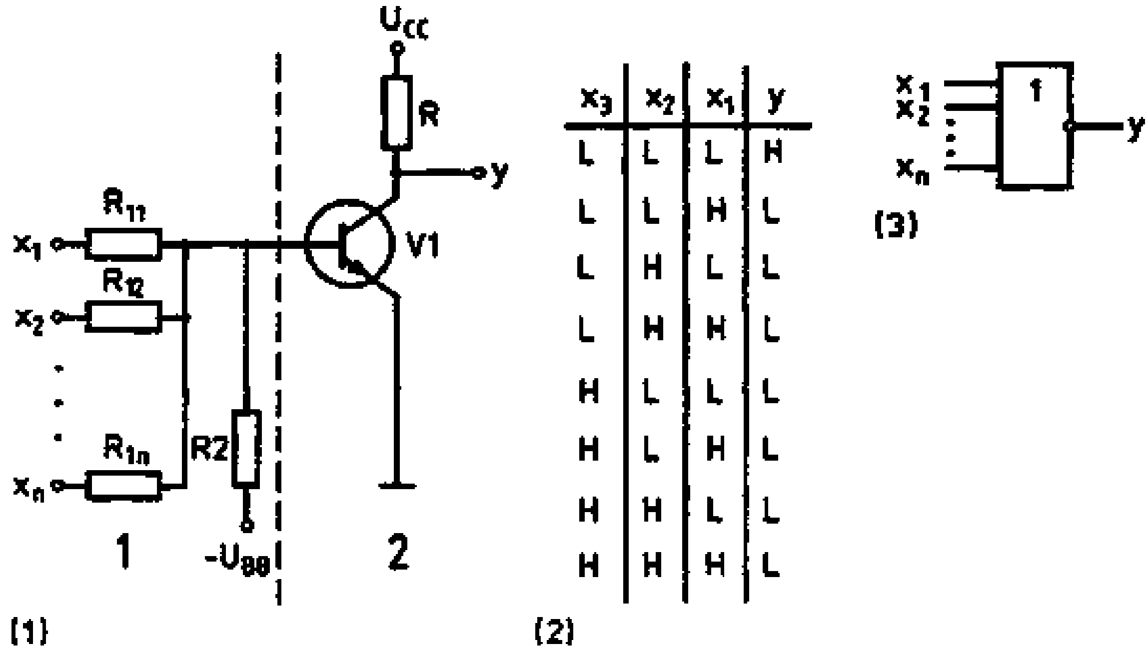
(1) not allowed for normal outputs
(2) allowed for open collector output

Especially in higher integrated circuits both output transistors can become high−resistive, that means they can be blocked by a special input. Now the output can take on a third state. Such outputs are called tristate outputs. They are employed if several circuits are connected as transmitter on a common line (bus). The unit load current corresponds to the input load factor (N_i = 1 (i input).

<u>NOR Interconnection</u>

A NOT − OR, which usually is called NOR, results from a combination of an OR interconnection with a negator (or NOR gate). The basis is an inverse gate. The input is extended by further resistors R_{11} ... R_{1n}. This is called fan−in.

While a NAND interconnection in resistor−transistor logic (RTL) is not possible since AND functions cannot be realized with resistors, a NOR interconnection is possible in RTL.



x_3	x_2	x_1	y
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

Figure 135 NOR element

(1) resistor−transistor logic circuit,
(2) truth table for three input variables,
(3) circuit symbol
1 OR element,
2 NOT element

Transistor V1 is connected through if H−level voltage occurs at least at one input. Then L−level voltage occurs at the output.

At the input of a NOR element H level dominates.

In general, this is expressed as follows:

$$y = x_1 \vee x_2 \vee \ldots \vee x_n = x_1 + x_2 + \ldots + x_n$$

(read: x_1 or x_2 or ... x_n not)

Figure 136 shows a NOR interconnection in diode−transistor logic. Compared with the resistor−transistor logic, its input decoupling is better.

The transfer characteristic is identical with that of Figure 130(3). This is obvious since the logic functions AND and OR, respectively are not described in this characteristic but only the negation which appears in NAND elements as well as in NOR elements.

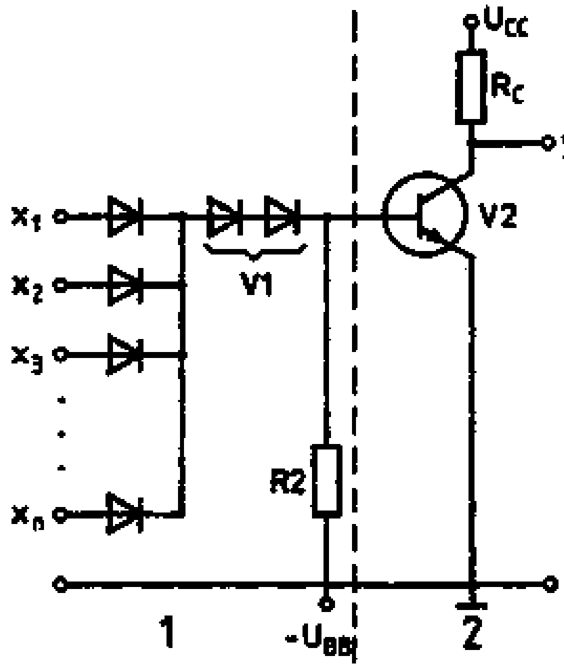


Figure 136 NOR element of diode−transistor logic

1 OR element,
2 NOT element

A particularly simple solution for a NOR element results from the addition of further parallel−connected transistors to the switching transistor of a MOSFET inverter. The transistors V1 ... V3, further transistors can be parallel−connected, have a common load resistance which is provided by V4. This solution is a transistor−transistor logic.

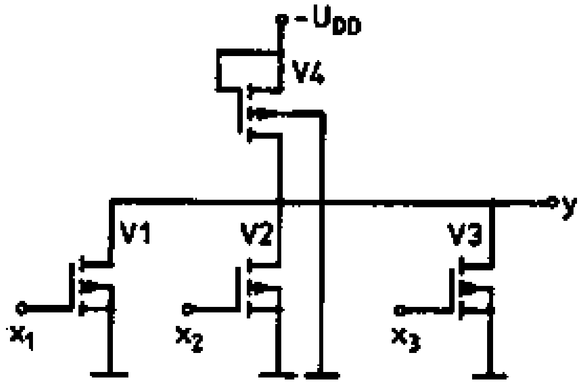


Figure 137 NOR element of transistor−transistor logic with MOSFET

On the basis of this NOR element, a number of circuits with p−channel MOSFET (enhancement) has been developed. They have been completed by several highly integrated circuits of n−channel technology and complementary design and form the basis for many industrial controls.

While p−channel types require negative operating voltage and function with negative logic, n−channel circuits are characterized by positive logic and can be interconnected with bipolar digital circuits. This is called TTL compatibility, because the H and L levels were first stipulated for TTL circuits of bipolar type. Therefore, the term TTL is firmly linked with bipolar digital circuits and never used for MOS circuits although they function in transistor−transistor logic as well.

The combinatory circuits described up to now function on the basis of overmodulation of the switching transistor in the "on" state. This so−called over−modulation technique is characterized by a simple design of the basic gate and relatively long switching times. If these switching times are to be shortened, the i current switching technique is applied instead of the overmodulation technique. Figure 138 shows its basic principle. According • to the switching state, a constant current flows through transistor V1 or transistor V2, respectively. A simultaneous current flow through both transistors is only permissible in the switching phase. This circuit is a differential amplifier but i uses only the final states (V1 blocked − V2 on or V1 on − V2 blocked).

The crucial point is the more positive input voltage. It connects through the respective transistor, whereas the other one blocks. This principle can easily be made clear by comparing the circuit with a two−armed lever balance (Figure 138(3)). As one side lowers, the other one rises. The pivot point of the lever is the fixed point. In the circuit, the fixed point is the emitter potential. If the bases of the transistors V1 and V2 have the same potential ($?_{B1} = ?_{B2}$), the current is divided equally on both transistors. This is used for differential amplifiers of analogue type. In digital systems the relationship is B1 ? B2, and thus applies U_{BE1} ? U_{BE2}. The current supplied by the power source is always divided accordingly on the transistors. In the desired extreme case $U_{BE1} > U_{BE2}$ or $U_{BE1} < U_{BE2}$ it flows completely through the on−state transistors. The same applies if one base current is kept constant as by application of a reference voltage in the current switching technique. For this reasons, signals inverted to each other can occur at the outputs y_1 and y_2 (Figure 138(2)) which are referred to as complementary signals.

Since the transistors are emitter−coupled, these circuits are classified as emitter−coupled logic (ECL). Switching times of about 1 ns can be achieved, compared with TTL that achieves. 15...80 ns and MOS circuits with more than 100 ns. Gates with short switching times are more sensitive to interference voltage, have a higher power input and require a higher edge steepness of the modulation signals. Therefore they should be used only if short switching times are required.

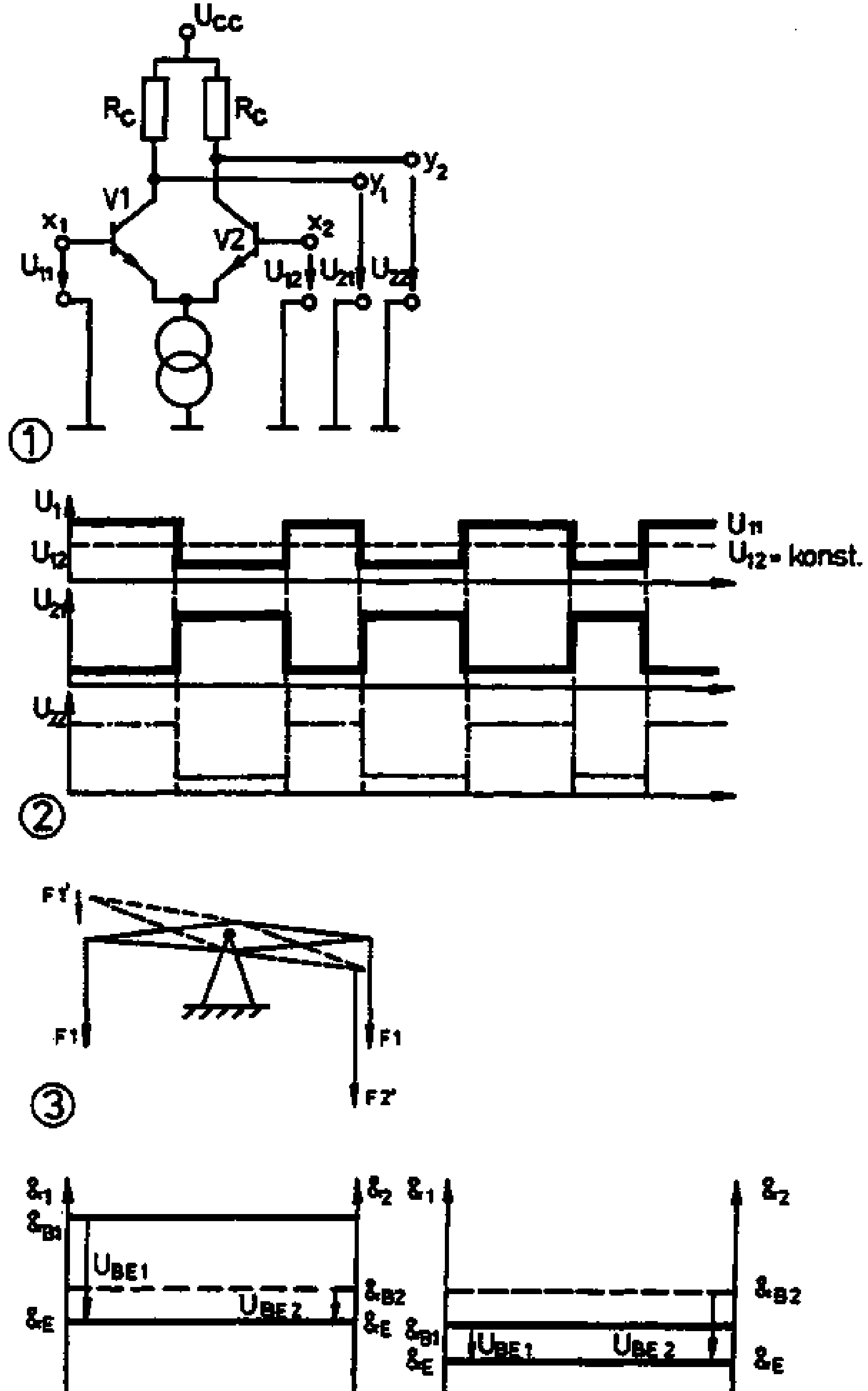


Figure 138 Current switching technique

(1) basic structure,
(2) pulse diagram,
(3) comparison with a balance,
(4) voltage relation with U_{BE1} U_{BE2} = const.,
(5) voltage relation with $U_{BE1} < U_{BE2}$ = const.

1.5.3. Sequential circuits

In sequential circuits, the output does not only depend on the actual state of the input, but also on the previous state of the output itself.

They are characterized by feedbacks of outputs to inputs and have a storage effect.

Circuit groups important to automation engineering are:

– triggers
– pulse shapers
– pulse generators.

Triggers:

A trigger is a circuit with two outputs and two stable states that are characterized by levels inverted to each other at . the outputs.

Such a layout is also called flipflop or bistable sweep stage. According to the kind of response to modulation, triggers are classified into

– static triggers and
– dynamic triggers.

Static triggers can be set during the whole width of the input pulse whereas dynamic triggers respond only to one edge of the input pulse. They are referred to as edge–triggered flipflops.

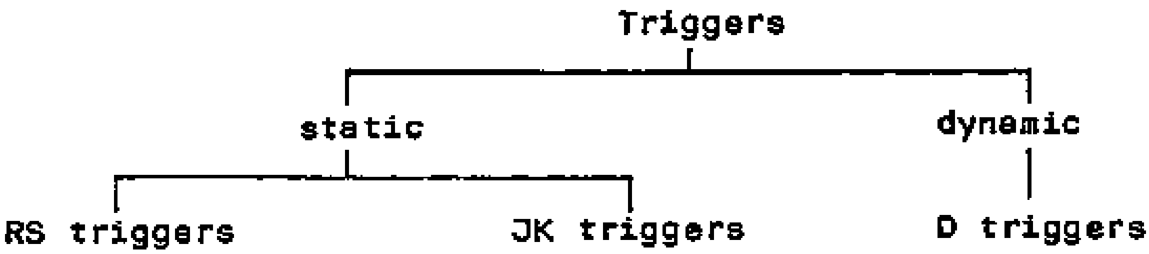


Table 12 Classification of triggers

RS trigger

The RS trigger has two inputs: R (reset) and S (set), and two outputs: Q and $\overline{Q}$, the levels of the same are always inverse. Figure 139 shows the basic circuit for an RS trigger. The symmetric lines in the figure separate the two NOR elements which are clearly shown in Figure 132 (2).

When switched on, the circuit has an incidental output state. In this state one transistor is conducting, the other one is blocked.

If V1 carries a current, its collector potential is about zero, V2 does not receive base voltage and is blocked.

The output voltage at Q is on L level and at $\overline{Q}$ on H level. The connection remains in this state, only a positive voltage (H level) at the input S can make transistor V2 conductive. With the current flowing through V2 its collector potential decreases, and transistor V1 changes to the off state. This happens very fast because of the feedback. The connection sweeps into the new stable state H at the output Q and L at $\overline{Q}$. This state remains (stored) until an H level at R triggers a new sweep.

The truth table (Figure 139(3)) shows the context. Index n signifies that nothing is changed at the output. An H–level voltage on both inputs at the same time leads to the forbidden state $Q = \bar{Q} = L$, that is in contradiction to the demand for negated output signals.

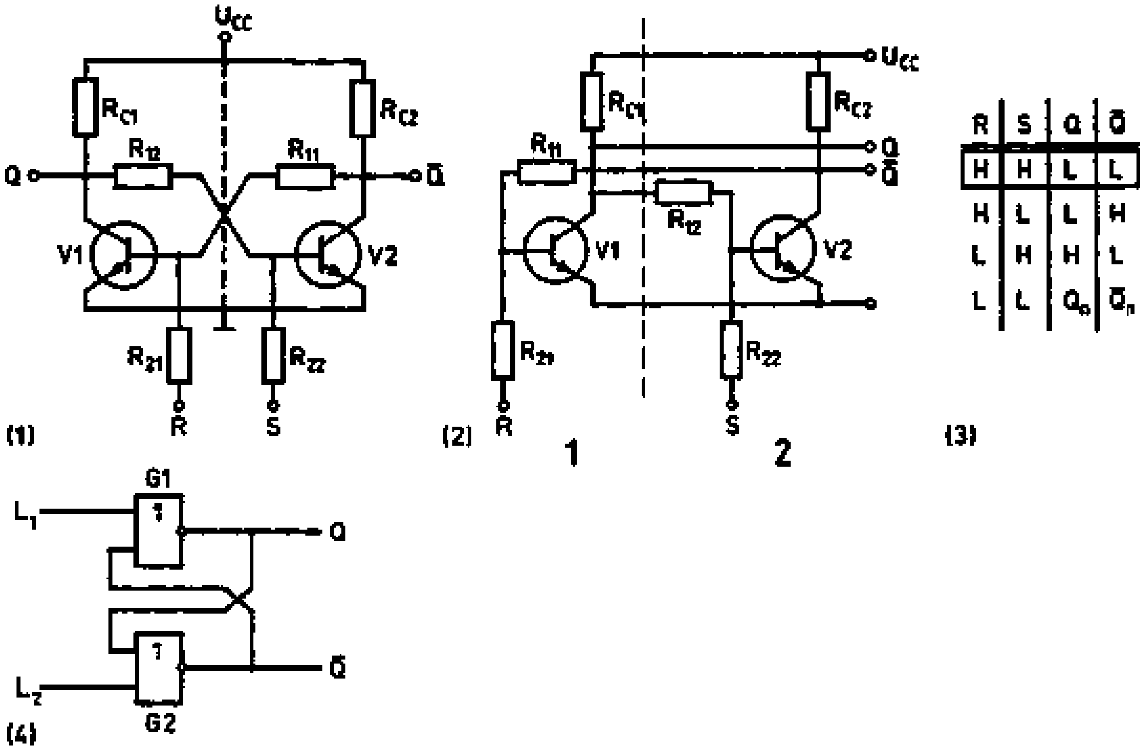


Figure 139 RS trigger

(1) basic structure,
(2) circuit of two cascaded NOR elements,
(3) truth table,
(4) basic structure with two NOR gates
1 NOR element 1,
2 NOR element 2

> The RS trigger does not allow H–level voltage on both inputs at the same time if the trigger consists of NOR elements. If it consists of NAND elements, L–level voltage simultaneously on both inputs is forbidden.

Figure 140 shows an RS trigger with NAND elements.

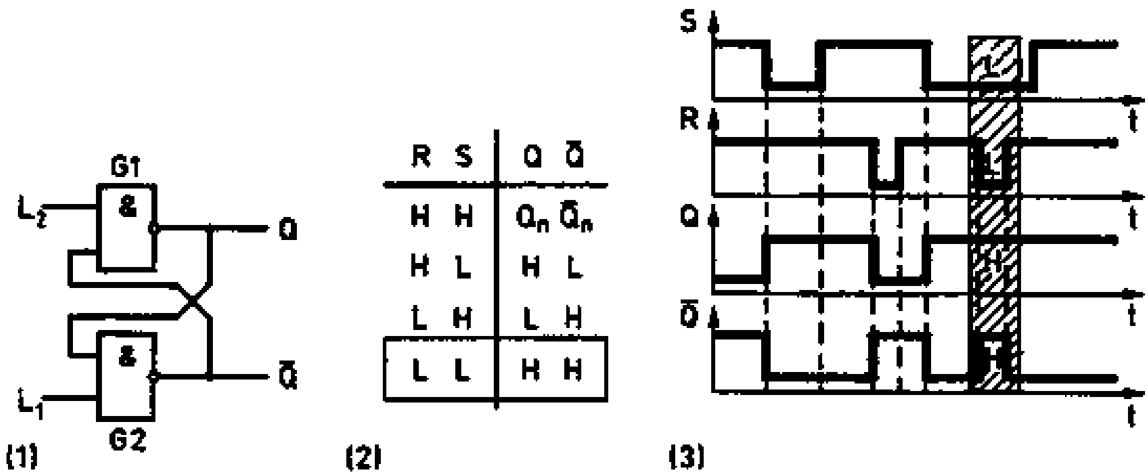


Figure 140 RS trigger with NAND elements

(1) basic structure,
(2) truth table,
(3) pulse diagram

Another disadvantage of RS triggers (they always respond to interference pulses) is diminished if the trigger is activated or released only at given moments. The result is a clocked RS trigger, the basic structure of which is shown in Figure 141. The information inputs R and S are on two additional NAND gates, G3 and G4, the second inputs of the same form together the timing input, more precisely, the releasing input. The normal trigger G1 and G2 is set by the negated information signals that can occur only if R and T or S and T a re on the H level.

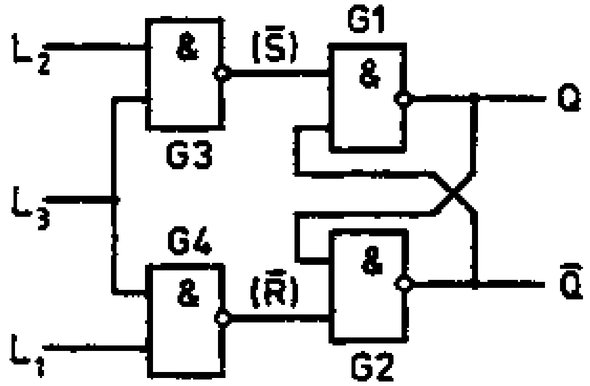
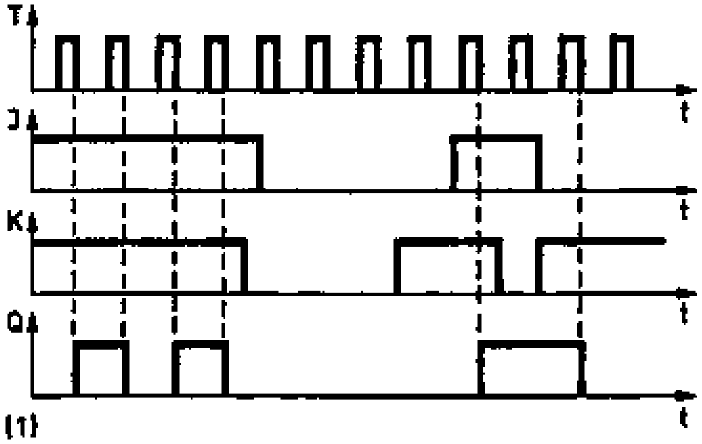


Figure 141 Clocked RS trigger with NAND elements

<u>JK Trigger</u>

The JK trigger is a clocked trigger, its information inputs are marked with 3 and K. Contrary to the RS trigger, input signals J = K = L are possible. The term JK has been chosen arbitrarily. Figure 142 shows the truth table and a pulse diagram. For the pulse diagram, some possible situations have been chosen.



t_n		t_{n+1}	
J	K	Q_n	$\bar{Q}_n$
L	L	Q_n	$\bar{Q}_n$
L	H	L	H
H	L	H	L
H	H	$\bar{Q}_n$	Q_n

(2)

Figure 142 JK trigger

(1) pulse diagram,
(2) truth table

A JK trigger switches the HL edge of the clock, the inputs J and K prepare the switching. Therefore they are called preset inputs. Normally there are several J and K inputs that are AND−interconnected. If the preset inputs are on H level the trigger switches over with each HL clock edge and can be used as frequency divider 1 : 2.

By means of the set inputs the trigger can be set independently of the clock state or the preset inputs. Here applies L at R sets Q on L or L at S sets $\overline{Q}$ on L.

Figure 143 hints these inputs only, they lead to all the eight gates.

Very often JK triggers consist of two clocked RS triggers. These are referred to as Master and Slave. If the clock input is on H level, the Master takes the data of 0 and K to the gates 3 and 4 where it stores them. With the HL edge and during the L−level clock period the Slave is released via Negator G9 and takes over the data from the Master. Gates 7 and 8 are set, and the outputs take on the respective potential.

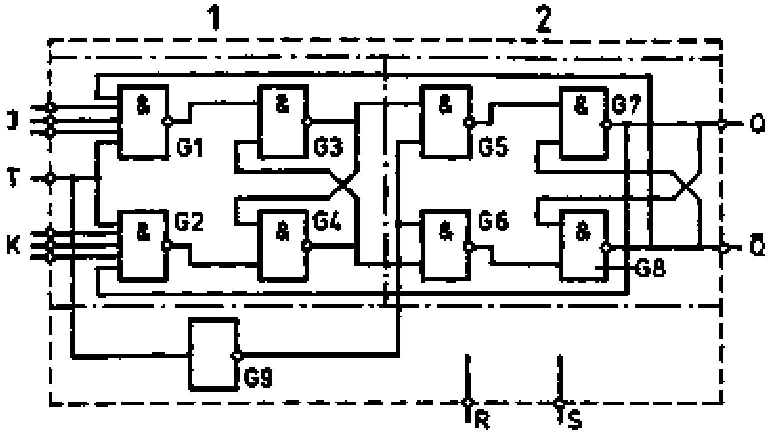


Figure 143 JK Master−Slave trigger

1 Master,
2 Slave

D Trigger

While the JK trigger can be set during the whole clock pulse time (H level), the D trigger is edge−triggered. Figure 144 shows that for the LH edge. This edge transfers the trigger at the output 0 into the state Q = D. D stands for delay since the state D occurs at the output only with the LH clock edge. Edge−triggering makes the trigger more insensitive to interferences. The trigger is used to synchronize operations with only one clock or to build up shift registers.

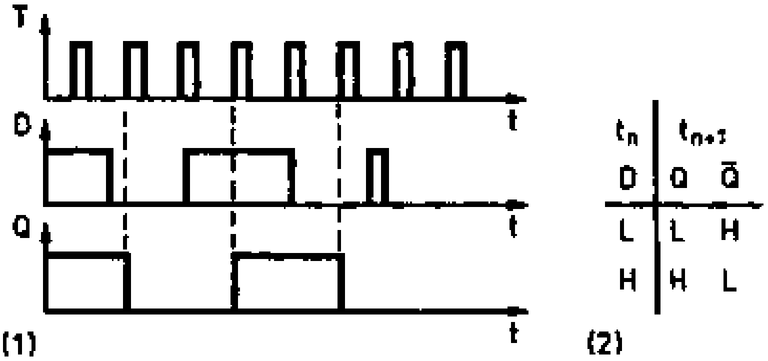


Figure 144 D trigger

(1) pulse diagram
(2) truth table

Pulse Shaper

When modulating digital circuits, the pulse form has to meet certain requirements. These are the amplitude A, the pulse duration t_i and the edge steepness. Figure 145 summarizes the important pulse parameters. The pulse duration t_i is measured at 70% of the amplitude. The rise time t_r (r rise) and the fall time t_f (f fall) are measured between 10% and 90% of the amplitude. The edge steepness that corresponds to the rise time or the fall time is also expressed as follows: $t_{LH} = t_r$ and $t_{HL} = t_f$. In principle applies $t_{HL} > t_{LH}$. If the required values cannot be achieved or guaranteed, a pulse shaper has to be employed that gives pulses of the standard values.

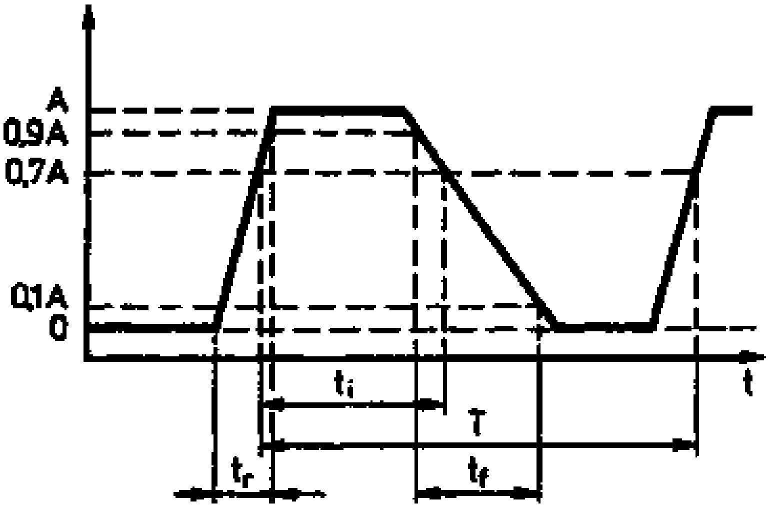


Figure 145 Definition of pulse parameters

Schmitt Trigger

The Schmitt Trigger is a threshold switch. At a certain input level the circuit sweeps rapidly into a H−level state at the output. With a lower input level it sweeps back into the normal state with L level at the output. The difference between the releasing input levels is referred to as hysteresis. The form of the input voltage is optional. The reason for the hysteresis is explained below. In Figure 146 the hysteresis $U_H = U_1 - U_2$.

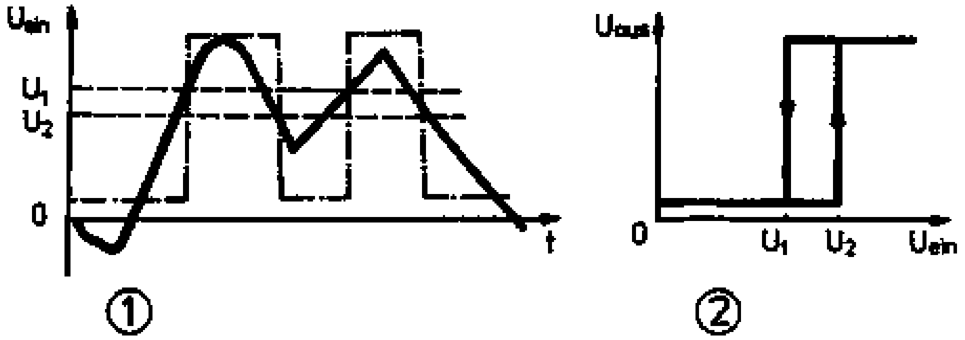


Figure 146 Operation of a threshold switch

(1) line diagram,
(2) transmision characteristic

Figure 147 shows the basic circuit of a Schmitt trigger. In the normal state ($U_{in} < U_1$) transistor V1 is blocked and transistor V2 conductive through R2, R3 and R4. The low voltage $U_{out} = U_{R6} + (U_{CE\ sat})_{V2}$ occurs at the output.

When U_{in} ? $U_1 = U_{R6} + 0.7$ V, V1 becomes conductive, the current flow causes a partial voltage at R2. The base potential at V2 decreases and V2 blocks. This process is supported by the feedback through the common emitter resistor and, therefore, it is very fast. When V2 is blocked, $U_{ouT} = U_{C6}$ occurs at the output.

When $U_{in} = U_2\ U_{R6}$, V1 blocks again, and the circuit returns to its normal state. This process, too, is supported by R6 and is also very fast.

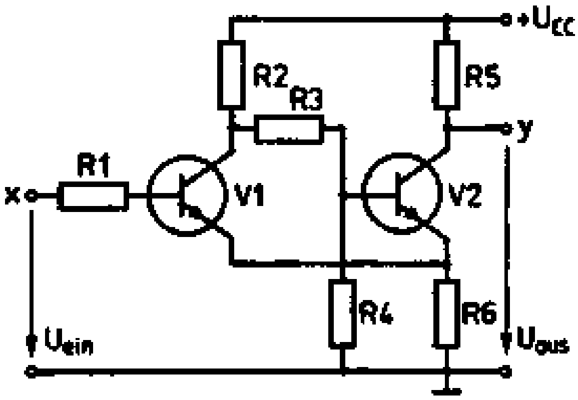


Figure 147 Schmitt trigger of discrete circuit type

The common emitter resistor R6 of the two transistors is decisive for the hysteresis. The bias point of transistor V2 is determined by the resistors R2 to R6. The transistor is over−modulated in the conductive state so that the output voltage does not become too high. That means that the transistor's base current is heavier than it would be necessary for the flowing collector current. Thus its bias point is nearly independent of the value of resistor R6. The switch−on threshold for V2 that corresponds to the voltage U_2 in Figure 146 depends only little on the R6 value. Because of $(I_C)_{V2}$, its voltage $U_{R6} = (I_C)_{V2}$ R6 is directly proportional to the resistor value and has a strong influence on the switch−on threshold of V1. This threshold corresponds to the voltage U_1 in Figure 146. With increasing R6 values U_1 rises and thus the hysteresis of the circuit, too. For R6 = 0 the hysteresis would be zero, too, but the circuit would not work.

The hysteresis is necessary for the regular operation of a Schmitt trigger. The smaller it is, the worse are the dynamic properties of the trigger.

A Schmitt trigger converts any input voltage into a square−wave voltage when the amplitude of the input voltage exceeds its switching threshold. It works as voltage discriminator.

Sweep stages

The term "sweep stage" describes the behaviour of a special amplifier circuit. Its output signal can have two values that correspond to the already known H or L level. The change−over from one value to the other one, usually referred to as states, is very fast. The circuit sweeps into the other state. I The sweep stages are classified according to the release of the sweep and the stability of the states. Regarding this stability, the following types are distinguished:

monostable sweep stage	− one stable stete
monoflop	one metastable state
monostable vibrator	
astable sweep stage	− no stable state
multivibrator	
astable vibrator	
bistable sweep stage	− two stable states
flipflop	
trigger	
bistable vibrator	

Monoflops are only used as pulse shapers. A monoflop shapes a pulse of defined duration. For this purpose, thw switching operation must be released by an input signal.

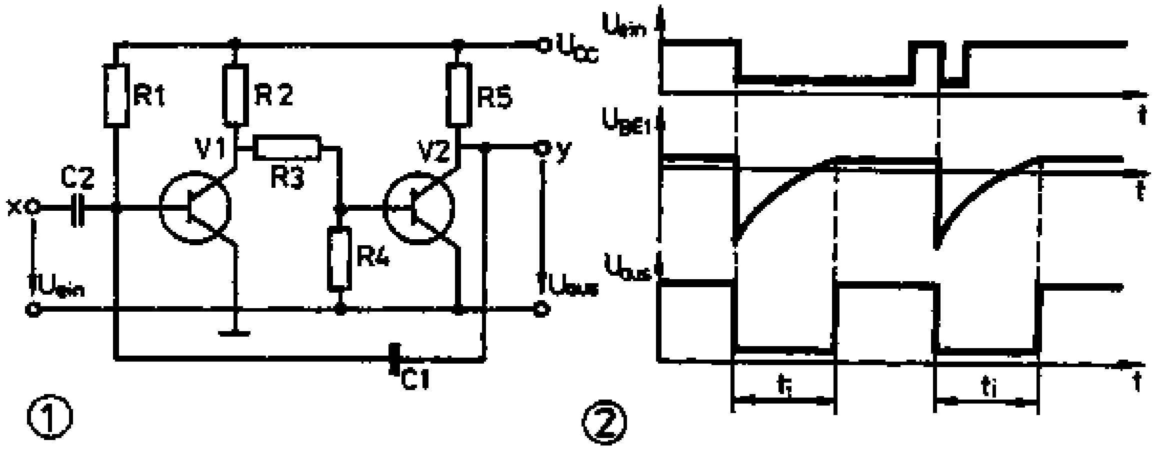


Figure 148 Monoflops of discrete circuit type

(1) basic circuit,
(2) pulse diagram

Figure 149 shows a circuit where, in the normal state, the I stable state, the transistor V1 is conductive and, because of the high partial voltage at R2 caused by its collector current, the base potential for V2 is as low as to make it block. Thus the working voltage, i.e. H level, is applied at the output. The I capacitor C1 is charged to about U_{cc} (Figure 149(1)).

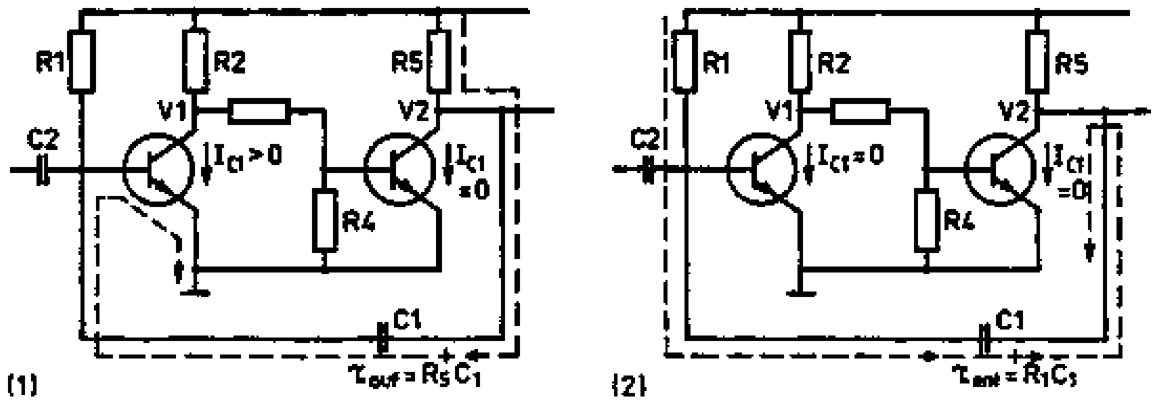


Figure 149 Operation of a monoflop

(1) stable state (C1 is charged),
(2) instable state (C1 is being discharged)

The circuit can maintain this state for any duration of time. Because of a negative voltage jump at the input, which is fully transmitted to the V1 base through C2 (the voltage cannot jump at a capacitor), V1 is blocked for a short time. The transistor V2 becomes conductive and the capacitor C1 is discharged through R1. The V1 base remains negative and V1 remains blocked (Figure 149(2)). Once C1 is discharged to an extent whereupon the V1 base becomes positive again, V1 returns to the conductive state and the circuit sweeps back into the initial state. The capacitor C1 is charged again through R5. The next release must not follow until C1 is charged again. The monoflop needs a recovery time t_R.

If the recovery time is shorter, the pulse duration t_i is shorter, too.

If the recovery time is maintained, t_i ? 0.7 R_1 C_1.

Figure 150 shows a circuit with NAND gates. It features a high ratio of pulse duration to recovery time. The standard values are:

R_C = 10 k?; R_W ? 330 ?; R_B ? 1 M?; h_{21e} = 100
t_i ? 0.7 R_BC
t_R ? 0.7 R_WC

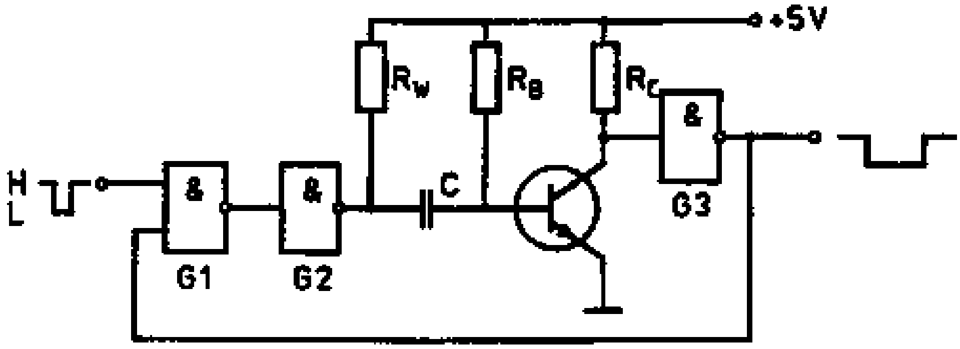


Figure 150 Monoflop consisting of NAND gates and an npn transistor

Hard rays, such as gamma rays or neutron rays but also cosmic or nuclear rays, are harmful to the functional units, particularly to semiconductor components. The most susceptible ones are bipolar transistors. The rays generate charge carriers and higher radiation powers irreversibly change the lattice structure of the material. The generation of charge carriers makes a bipolar transistor temporarily inoperative, the change of the lattice structure destroys it.

While with unipolar transistors the generation of charge carriers is not harmful, the change of the lattice structure destroys them, too. Consequently MOS transistors are less susceptible to radiation than bipolar transistors.

Electronic tubes are even more resistant to hard rays. Still today they are superior to semiconductors in this respect.

<u>Pulse generators</u>

Modulation of circuits, e.g. by clock pulses, calls for generators which send successions of pulses of about square form. The generators are called "pulse generators". The pulse generators mostly used are astable vibrators. The astable vibrator, also called multivibrator, is a two−stage feedback amplifier. Because of a high feedback coefficient (regenerative or positive feedback coefficient to be more exactly), the transistors get overmodulated and approximate square−wave voltage occurs at the outputs.

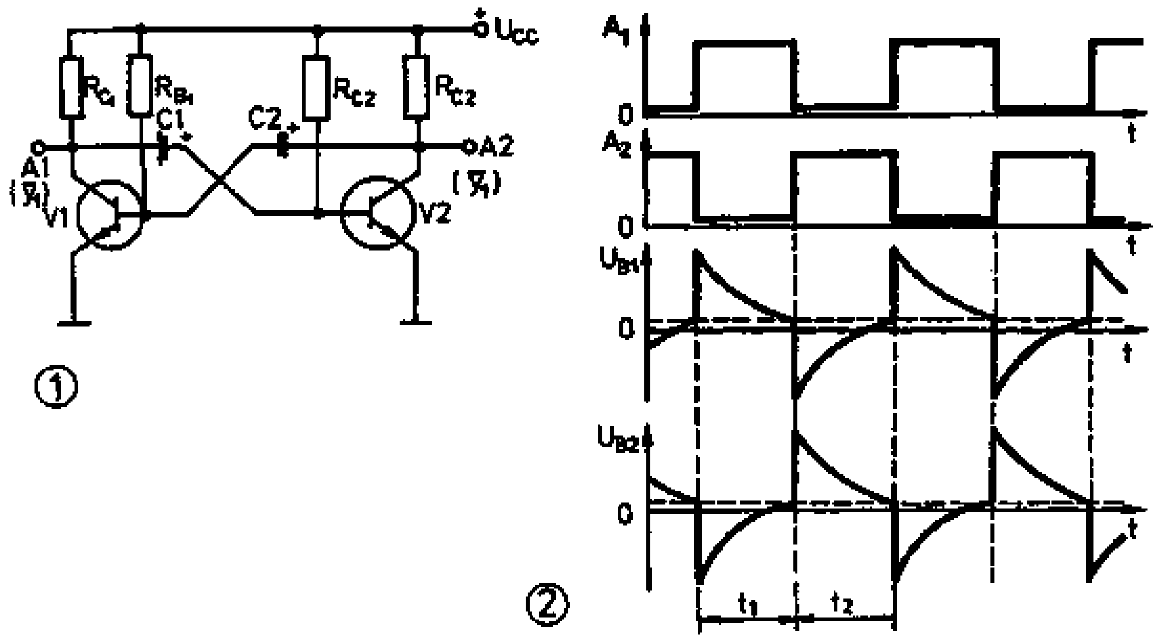


Figure 151 Astable vibrator

(1) basic structure,
(2) pulse diagram

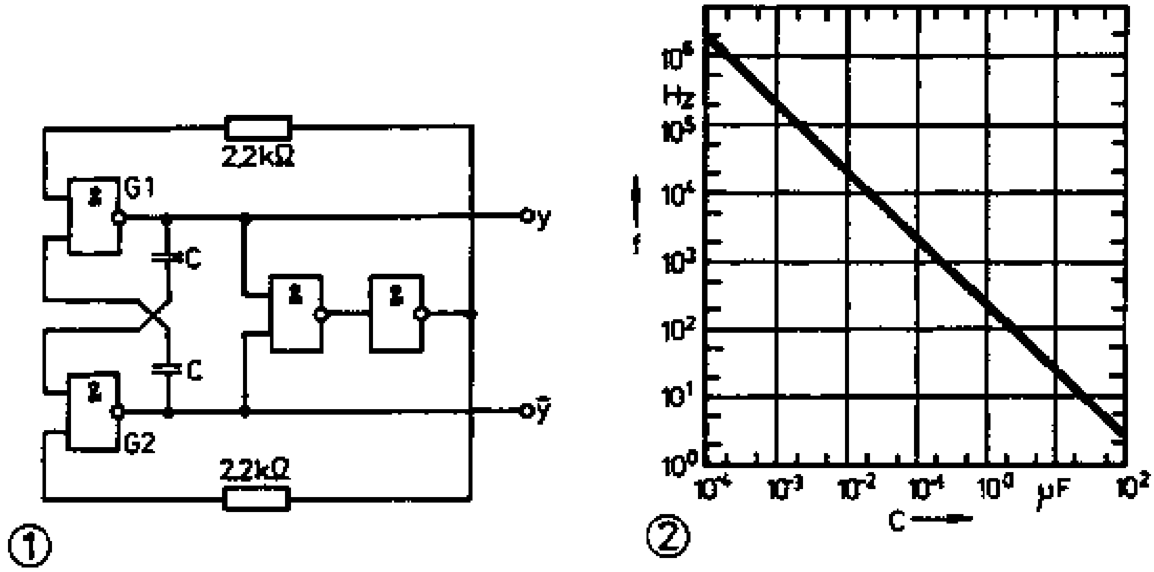


Figure 152 Astable vibrator with NAND elements

(1) basic structure,
(2) dependence of frequency on the capacitance

The 4−NAND−gate pulse generator according to Figure 152 features a wide oscillation frequency range. The gates G3 and G4 are used for amplification and facilitate starting of oscillation.

Counters, dividers and decoders

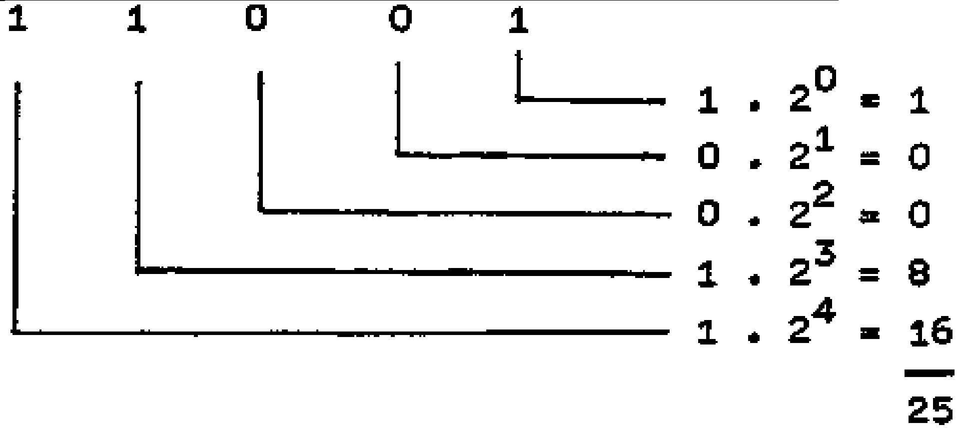
Counting operations are of great importance in automation engineering since the number of pulses or pulse trains is directly related to a technological process. Counting is dual (binary). Each binary number, which is also called "code word" in this connection is correlated with a decimal number. The correlation is shown in a truth table, based on the counter code, Out of the many known codes, the dual code (binary code) and the 8−4−2−1 code are widely used.

The dual code is the simpliest code at all. Beginning from the right, the digits have the valence of the power of two. This is shown in table 13 for the numbers 0...31 with 1 meaning that the power is existing and 0 meaning that the power is not existing.

Table 13 Examples for the binary code

2^4	2^3	2^2	2^1	2^0	decimal number	2^4	2^3	2^2	2^1	2^0	decimal number
0	0	0	0	0	0	1	0	0	0	0	16
0	0	0	0	1	1	1	0	0	0	1	17
0	0	0	1	0	2	1	0	0	1	0	18
0	0	0	1	1	3	1	0	0	1	1	19
0	0	1	0	0	4	1	0	1	0	0	20
0	0	1	0	1	5	1	0	1	0	1	21
0	0	1	1	0	6	1	0	1	1	0	22
0	0	1	1	1	7	1	0	1	1	1	23
0	1	0	0	0	8	1	1	0	0	0	24
0	1	0	0	1	9	1	1	0	0	1	25
0	1	0	1	0	10	1	1	0	1	0	26
0	1	0	1	1	11	1 .	1	0	1	1	27

0	1	1	0	0	12	1	1	1	0	0	28
0	1	1	0	1	13	1	1	1	0	1	29
0	1	1	1	0	14	1	1	1	1	0	30
0	1	1	1	1	15	1	1	1	1	1	31



Example:

The code is suitable for arithmetic operations but has the disadvantage that the numbers easily get very long. The 8 – 4 – 2 – 1 code can represent the decimal numbers from 0...15. It is used for coding of the decimal numbers from 0...9 and is then called "BCD code" (binary–coded decimal number).

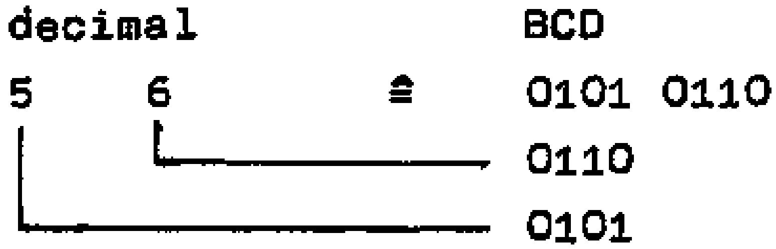
<u>Table 14</u> Examples for the BCD code

8	**4**	**2**	**1**	**decimal**	**8**	**4**	**2**	**1**	**decimal**
2^3	**2^2**	**2^1**	**$2°$**	**number**	**2^3**	**2^2**	**2^1**	**$2°$**	**number**
0	0	0	0	0	1	0	0	0	8
0	0	0	1	1	1	0	0	1	9
0	0	1	0	2	1	0	1	0	10
0	0	1	1	3	1	0	1	1	11
0	1	0	0	4	1	1	0	0	12
0	1	0	1	5	1	1	0	1	13
0	1	1	0	6	1	1	1	0	14
0	1	1	1	7	1	1	1	1	15

Four binary digits are required to represent the ten figures from 0 to 9.

$2^3 = 8$ cannot represent the set (0...9). Using four digits, $2^4 = 16$ words can be formed. Since each word consists of four digits, it is called a "tetrad" (Greek: tetra = four).

To represent the figures 0 to 9, the first ten only of the 16 tetrads are used. The remaining tetrads 10 to 15 are called "pseudotetrads" (Greek: pseudo = false). For decimal numbers consisting of several digits, one tetrad is required for each digit.



Example:

A single−digit binary number can be stored by a trigger where each output, as well−known, may have the level H or L. When several triggers are connected in a chain, a counter is formed, the counting capacity "m" of which depends on the number "n" of triggers.

$m = 2^n$

A counter consisting of n triggers can count from 0 to m−1 since one digit is covered by the initial state.

Figure 153 shows a dual counter consisting of four JK triggers. Its counting capacity is $2^4 = 16$, i.e. it can count from 0 to 15 = m − 1. The states of the individual triggers are shown in the pulse diagram.

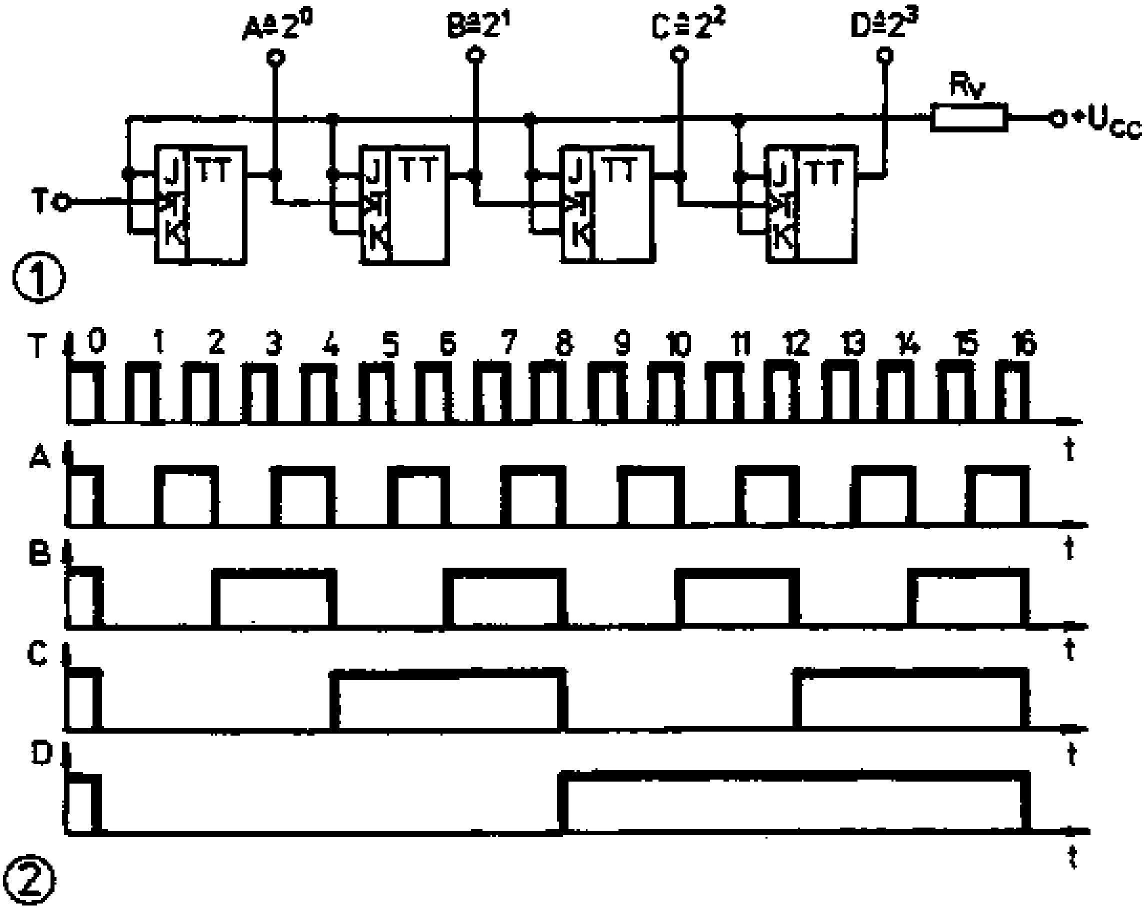
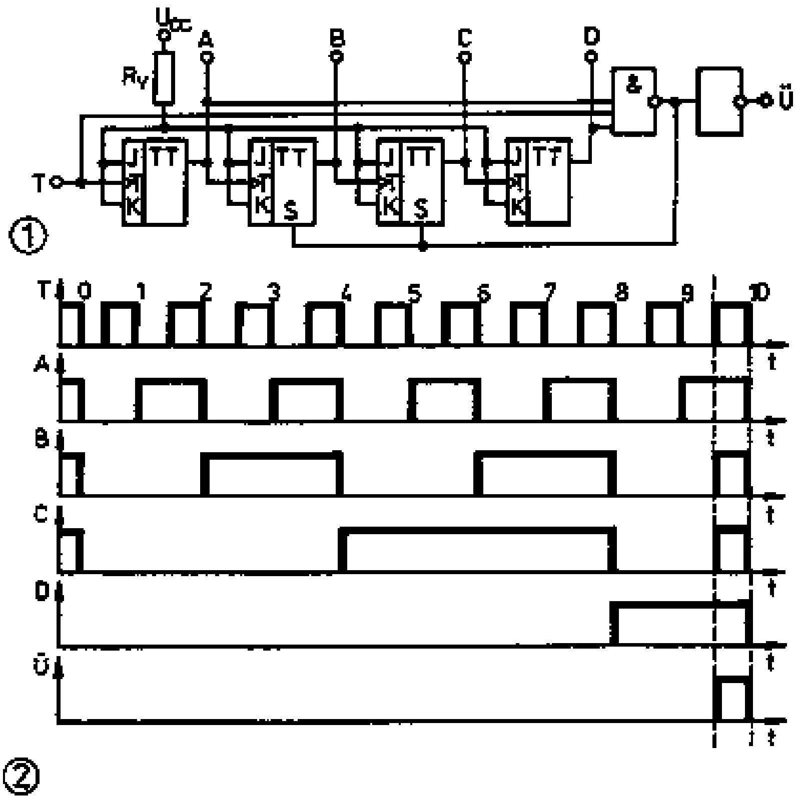


Figure 153 Dual counter with JK trigger

(1) basic structure,
(2) pulse diagram

The triggers trigger each other successively when the corresponding number of clock pulses has reached the input. This mode of operation is called "asynchronous". With a synchronous counter, all clock−pulse inputs are in parallel as shown in Figure 154. When the steps 10 to 15 are skipped by suitable feedbacks, a decimal counter is formed.



③

X	D	C	B	A	Ü
0	L	L	L	L	L
1	L	L	L	H	L
2	L	L	H	L	L
3	L	L	H	H	L
4	L	H	L	L	L
5	L	H	L	H	L
6	L	H	H	L	L
7	L	H	H	H	L
8	H	L	L	L	L
9	H	L	L	H	L
	H	H	H	H	H
10	L	L	L	L	L

Figure 154 Decimal counter with ID triggers

(1) basic structure,
(2) pulse diagram,
(3) truth table x state

This function can be performed by a simple circuit using the set input and an additional NAND gate. The advantage is that the –counter states correspond to the BCD code. With the tenth clock pulse (counting pulse) the triggers B and C are set to H, which results into an intermediate state – marked (2) and (3) in Figure 154 – corresponding to the number 15 acc. to the BCD code. The HL edge of the same clock pulse sets the counter to 0.

The triggers can assume the intermediate state because they can be set through the S or R input independently of the clock rate. The resistors R_V in the Figure 153 and 154 are intended for current limitation of the interconnection inputs D and K at U_{cc}. These resistors are not necessary if U_{cc} = SV is protected. Figure 155 shows the basic layout of a synchronous counter. Many interconnections are required which additionally load the trigger outputs. But synchronous counters have a higher counting frequency than asynchronous counters.

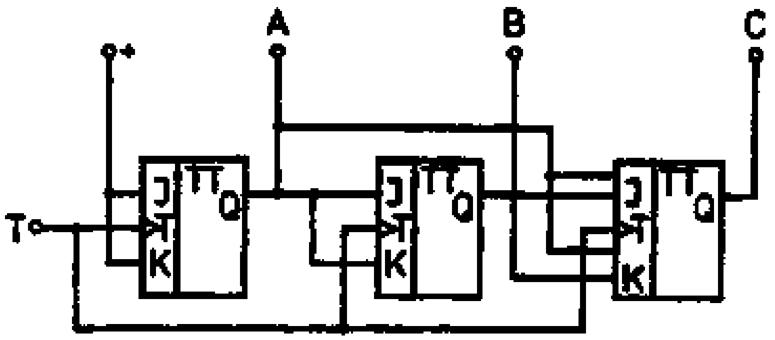


Figure 155 Synchronous counter for binary code

When several triggers are connected in a chain which is closed as shown in Figure 156, it is a ring counter (or closed counting chain). It features a very simple layout and uncoded operation but needs one trigger for each counting step.

Because of the feedback from the last to the first trigger, any data entered (0 or 1) circulates in the counter and is transferred by one position with each cycle. Ring counters can be advantageously used in automation processes where a certain sequence of steps shall be automatically performed after release, The clock rate can be adapted to the requirements of the process and need not be periodic. (Figure 156(3))

Basically each counter can also be used as divider because the input pulses occur divided by the factor 2^n at its last output. The intermediate outputs are not required then. Any trigger may be used as 2 : 1 divider. This is shown in Figure 157 for the D trigger. Thus a pulse train of almost exactly the pulse duty factor of $t_1 : t_p = 1 : 1$ can be generated from a pulse train of any duty factor. (Figure 156 (2))

Decoders are required to convert the internal counter states into decimal numbers again or to drive a seven−sequent display, for example.

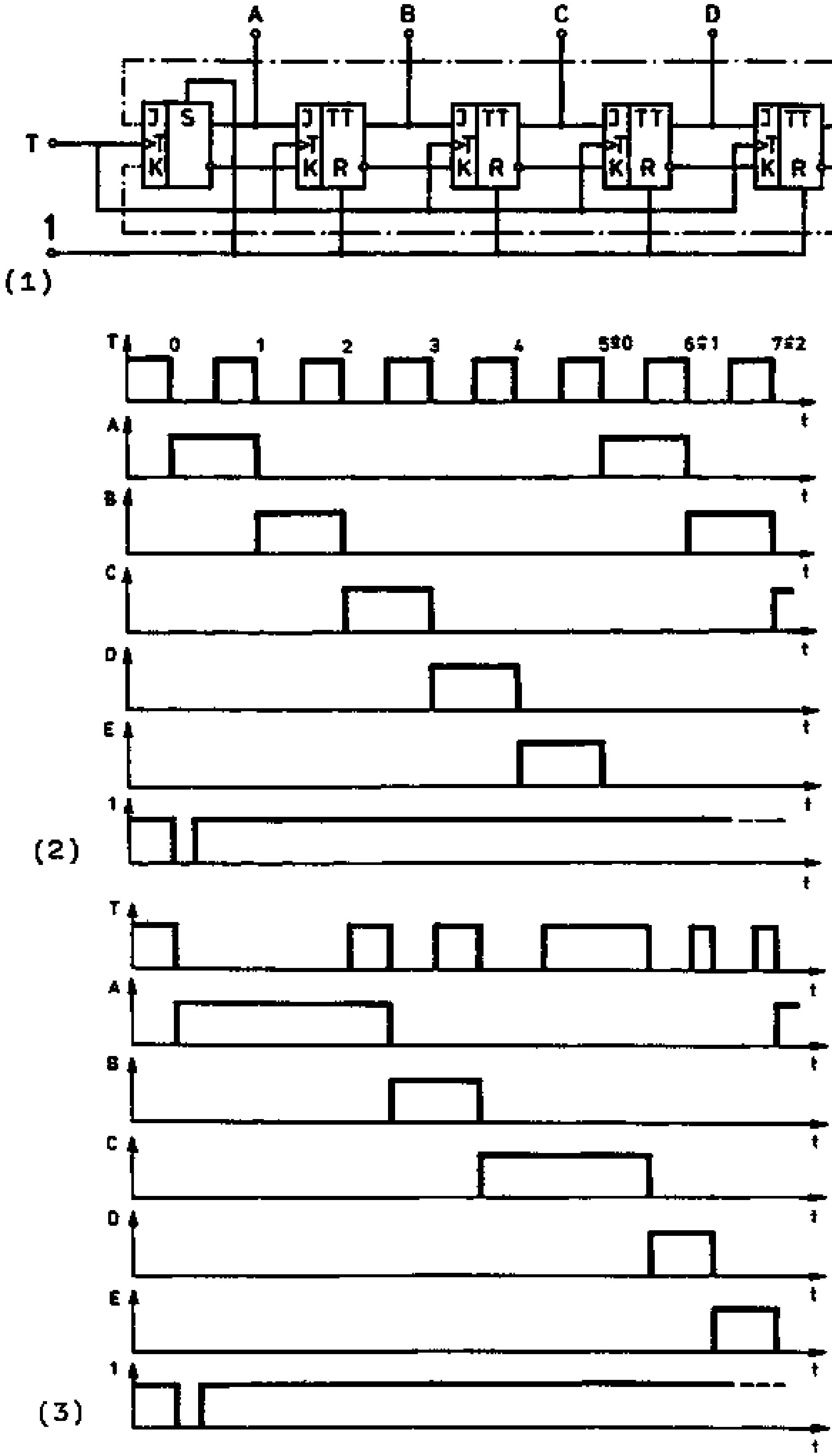


Figure 156 Ring counter

(1) basic structure,
(2) pulse diagram for periodic clock cycle,
(3) pulse diagram for aperiodic clock cycle
1 digits.

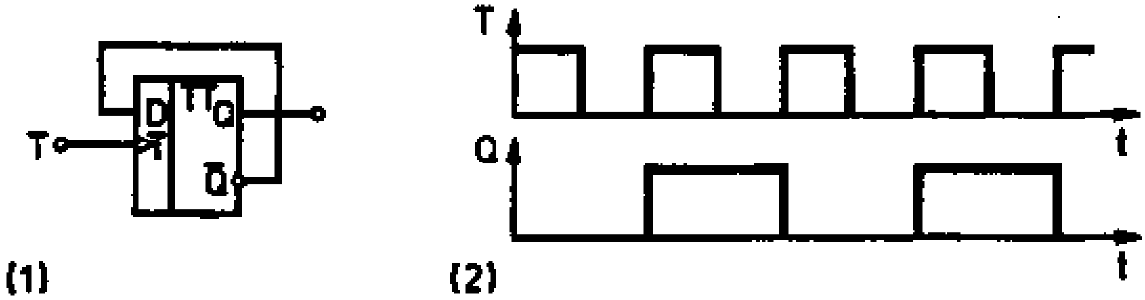


Figure 157 Binary divider with one D trigger

(1) basic structure,
(2) pulse diagram

The circuits are relatively sophisticated and in various layouts used for various purposes. The truth table as per table 15 shows decoding from the 8−4−2−1 code into i from 10.

Table 15 Truth table for decoding of the 8−4−2−1 code

Inputs				Outputs									
D	**C**	**B**	**A**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

A possible layout of a NAND−gate circuit is shown in Figure 158. It is an especially simple and clear arrangement because the negated values $\overline{A}$ ... $\overline{D}$ are also used. It uses eight quadruple NAND, one triple NAND and one double NAND. The combination into one decade circuit is economical here.

For modulation of a seven−segment display, one circuit is required. It decodes from the 8−4−2−1 code.

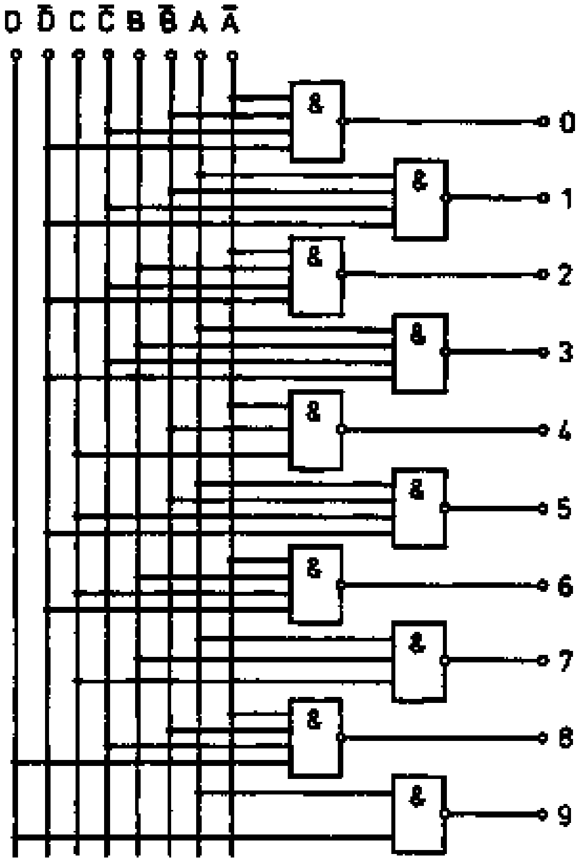


Figure 158 Example of a decoder with NAND gates

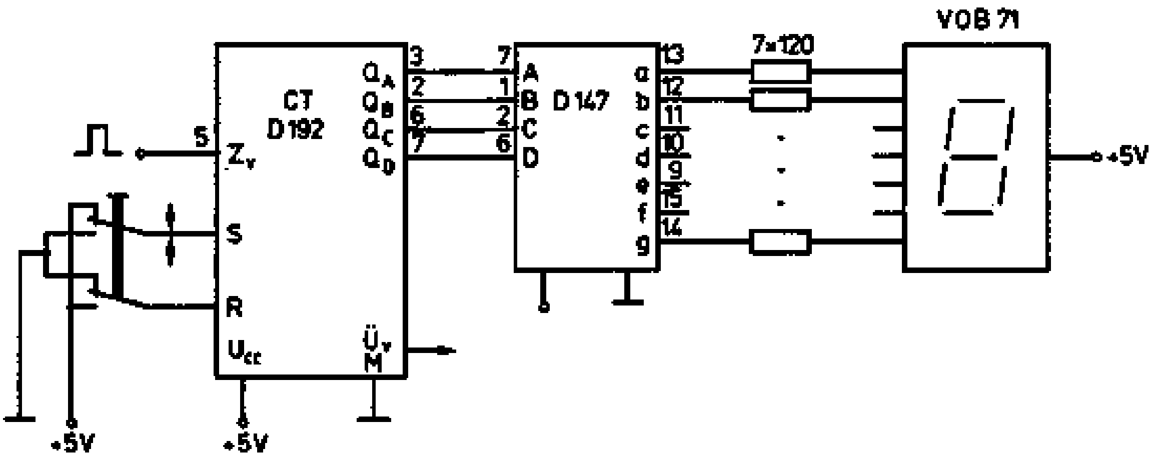


Figure 159 Example of the basic configuration of a decimal counter with TTL circuits

A counter stage with decoding for one decade can be arranged together with a counter circuit. A MOS circuit includes, in addition to the counter and decoder, also an intermediate store. This permits storage and display of a counter result while the counter goes on counting. Direct driving of counters by contact elements, such as relays, keys of switches, often result in faulty switching. The contacts vibrate when opening and closing thus performing several opening and closing operations. This is called "bouncing" or "chattering" of the contacts. Because of the short switching time the counters can follow such chattering operations and count incorrectly. The chattering effects can be completely eliminated by the use of an RS trigger. At the first contact touch the trigger switches to a stable state which is not changed by any further contact closing at the same gate input. The circuit is called "chatter−proof circuit."

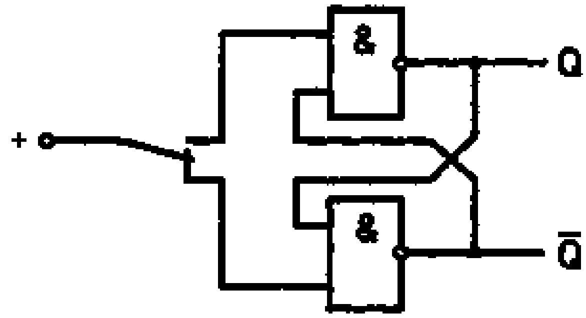


Figure 160 Chatter–proof circuit

Interface

Interface circuits have the following functions:

– adaption of external loads (outside the logic system)
– level adaptation at the transition to another logic system.

In the first case they operate as current amplifier or current driver and can drive, for example, relays, lamps or other elements of display devices.

Level adaptation is particularly applied for transitions from the MOS logic to TTL and vice versa.

Current drivers

Any circuit can deliver and receive only low current intensities. The current intensities, but also the supply voltages for the loads, can be considerably increased by downstream transistors. Figure 161, for example, illustrates the activation of a magnetic drive with TTL level. The diode V3 acts as zero diode against overvoltages when switching off. The drive switches on at H level at the gate output.

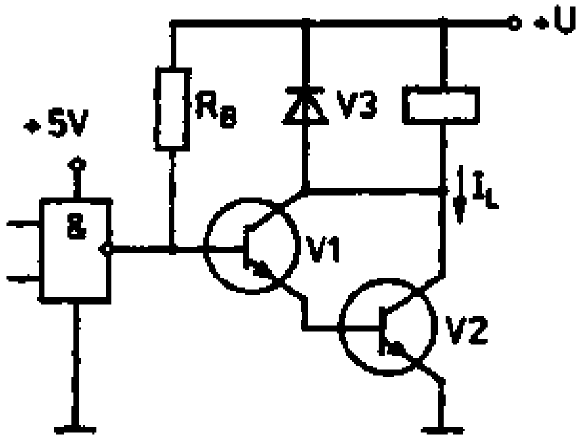


Figure 161 Current driver for TTL gate

Using a power transistor as V2, for example, currents up to 20 A at U_{CC} = 80 V can be switched. The transistor V1 must supply the base current necessary for this. The protective base resistor is calculated to the equation

$$R_B = \frac{U_{CC} - 1.4V}{I_L} B_1 \cdot B_2.$$

B1 current amplification of transistor V1
B2 current amplification of transistor V2

When an incandescent lamp is used as indicator, the problem is its low initial resistance which results in high current peaks at the moment of circuit closing. Figure 162 illustrates how this effect can be reduced. The capacitor (Figure 162(1)) delays the circuit closing process, the resistor (Figure 162(2)) preheats the incandescent lamp. Energetically preheating is unfavourable and causes heat problems when too many lamps are combined in one section.

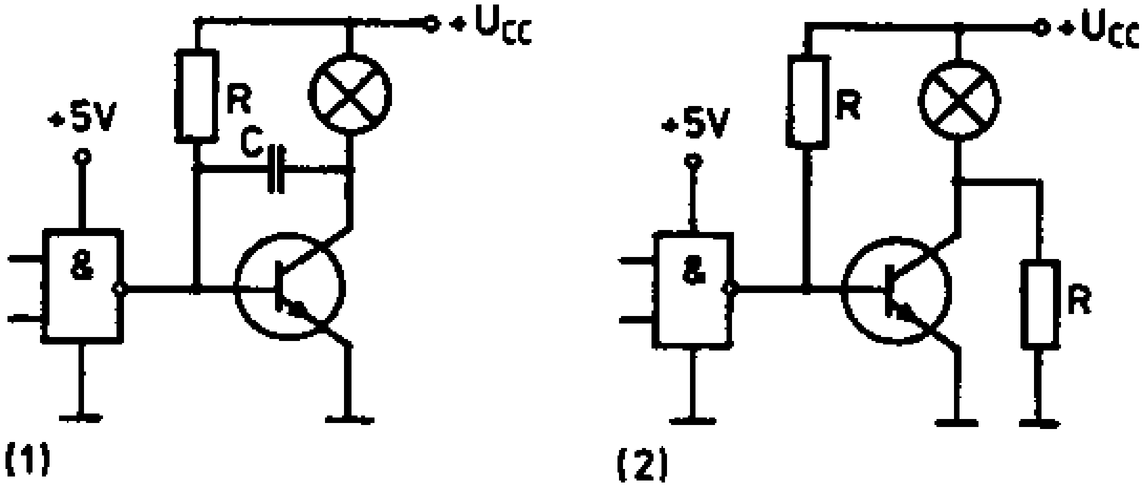


Figure 162 Prevention of current peaks when switching on incandescent lamps

(1) by means of a capacitor "C",
(2) by means of a resistor "R"

Level adaptation

The following circuits have proved to be useful for level adaptation:

– TTL ? MOS logic (Figure 163(1))
– MOS logic ? TTL (Figure 163 (2))

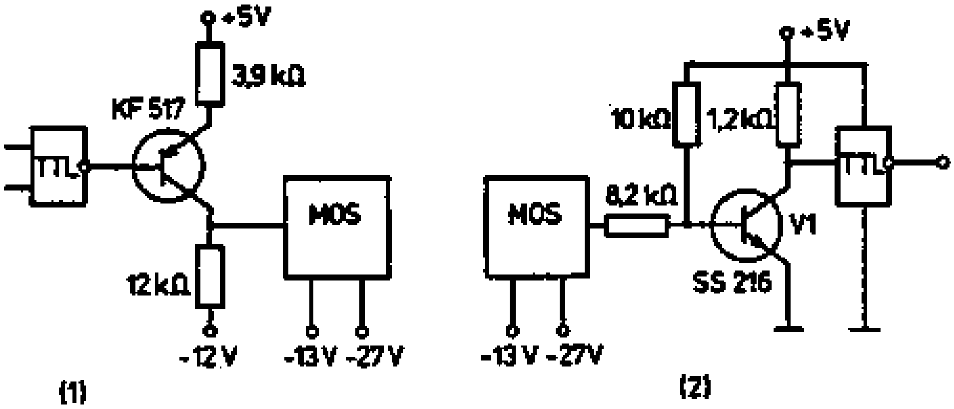


Figure 163 Level adaptation

(1) TTL – MOS logic,
(2) MOS logic – TTL

The two circuits use a transistor the supply voltage of which is selected so as to meet the conditions for the L and H levels of the circuit family to follow. This is explained by means of the example of TTL–MOS logic adaptation (Figure 163(1)).

With the H level at the output of the TTL gate the transistor V1 is conductive and its collector has a voltage of U~0 V. The H level of the TTL gate corresponds to the logic state 1 (positive logic) and causes an H level at the MOS gate which corresponds to the logic state "0" (negative logic).

An L level at the TTL gate blocks V1 with a voltage $U = U_{CC} = -12$ V at its output which is within the level range for L signals of p–channel high–voltage MOS gates. High voltage in this connection refers to the relatively high supply voltages for this circuit family. So the circuit adapts the levels and converts positive into negative logics. This makes clear again the purpose of an interface circuit to meet the conditions of the relevant system. With the conversion of MOS Logic into TTL according to Figure 163(2) the situation is the same but in the opposite way.

An L level at the output of the MOS circuit, which corresponds to the voltage U ? – 9 V and the logic state "1", blocks the transistor V1. Its collector features a positive voltage which is converted by a TTL inverter into an

"0" signal complying with the system which corresponds to the L level.

The MOS H level with U_H ? – 2 V cannot block the transistor V1, it is activated through the positively connected 10 k? resistor until saturation. Then its collector voltage is about 0.2 V, the output of the TTL inverter features the H level for positive logic.

2. Trouble shooting with electronic subassemblies

2.1. Definitions and requirements

In the event that constructionally determined technical data of a subassembly are not or no more achieved, so the faulty part is detected by means of suitable methods and means. In this case it makes no difference whether the fault occurs constantly or occasionally. Before trouble shooting it is to be decided, whether the expenditure of repair is worthwhile or the subassembly must be completely replaced.

The trouble shooting is to be carried out only to the extent that is necessary for the repair (i.e. a capacitor is not to be opened as it cannot be repaired).

<u>Occurrence of faults</u>

These may occur by

– manufacturing defects, such as

- component defects
- assembly defects in the manufacture of the subassembly (e.g. wrong connections, use of wrong components, defective or unsuitable mounting tools, technological defects),

– improper handling/transportation, such as

- mechanical damage,

– wrong use/operation, such as

- improper use of the subassembly (e.g. in aggressive environment, excessive vibrations)
- overload (e.g. excessive connected loads)
- bad maintenance (e.g. contaminated, no replacement of wearing parts),

– wear, such as

- aging (electrical components)
- wear and tear (mechanical components)

<u>Prerequisites for trouble shooting</u>

– Necessary knowledge of trouble shooter

- fundamentals of electrical engineering
- reading of circuit diagrams
- experience in trouble shooting
- handling of testing and measuring tools
- safety regulations

– Special knowledge of subassemblies

- mechanical construction
- electrical construction
- function
- purpose of application
- technical data

– Preparation of the defective subassembly

- cleaning from dirt and oil (with dust brush, vacuum cleaner or solvents)

Toxic gases may occur when using solvents. There is a danger of explosion when using naphtha.
A disassembly should be made only as far as it is necessary for trouble shooting.

<u>Instruments for trouble shooting</u>

– Testing and measuring tools (standard equipment)

- multirange meter for current and voltage with as high internal resistance as possible

- oscilloscope

- R–L–C measuring instrument

- transistor tester

- measuring instruments for specific subassemblies (signal transmitter, plug–in unit tester and others)

When switching–on a measuring instrument, the technical parameters and changes occurring in the circuit must be observed.

Figure 164 shows the measuring errors if the measuring instrument is wrongly used (for a correctly functioning subassembly the measuring result to be expected is 1 V).

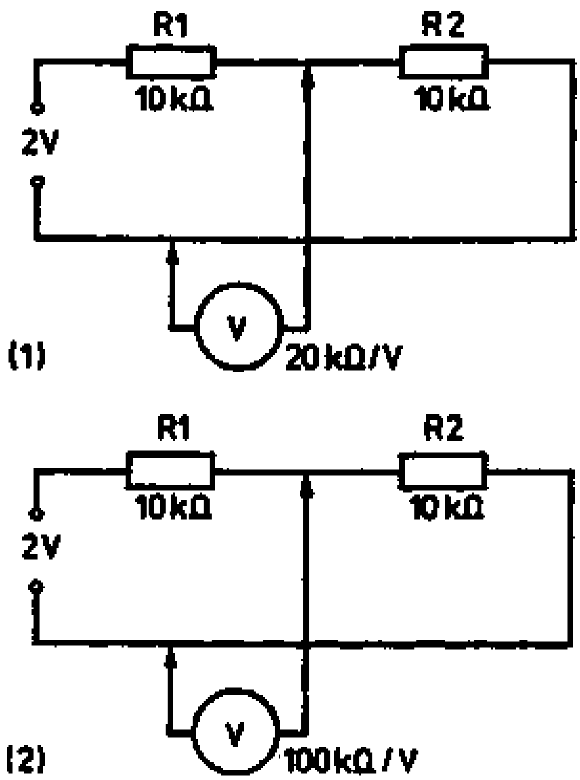


Figure 164 Selection of a voltmeter

(1) R1 is too low,
(2) R1 is correct

When a multirange meter with internal resistance of 20 k?/V is used, a voltage of about 0.8 V only is indicated for a correctly functioning subassembly.

This measuring error is the result of bridging the resistance R2 (10 k?) with the internal resistance of meter movement (approx. 20 k?).

When a measuring instrument with an internal resistance of 100 k?/V is used, a value of 0.95 V is already indicated.

The correct use of the measuring instrument is also featured by the accuracy of the measuring instrument.

The measuring instrument used must operate with a higher accuracy compared with the value to be measured. Measuring instruments are not used with highest but with the necessary accuracy.

– Hand tools (standard equipment)

• soldering device (possibly unsoldering device)
• screw drivers with insulated handles
• pliers with insulated handles
• spanners (above all socket spanners)
• tool specific to subassemblies, alignment tools, test cords, clamps

– Technical documentation

• Circuit diagram
shows the functional sequence within the circuit as well as all current paths and circuit sections.

Functional sequence: from left to right or downward. The measuring values and alignment points, the marking of components and their electrical values are partly included.

• Wiring diagram
serves to quickly locate the components and measuring points, It shows the true location of components within the subassembly.

• Test specification

It determines the test methods, test conditions, testing devices and test results. Test specifications should be available for all electronic subassemblies.

• Signal flow diagram
The transfer elements are shown in a scheme. It serves to control the signal flow. It is used for extensive subassemblies (such as electronic computers) where, possibly, circuit diagrams are too intricate.

• Functional description

It includes a detailed functional description of the sub−assembly (prerequisite to trouble shooting),

• Trouble shooting instruction

It includes specific advices as to certain fault effects and their causes and proposes special methods of trouble shooting.

• Reference books
technical books, technical journals, handbooks for components, self−made

fault files, trouble−shooting charts

– Other auxiliaries

• Inspection overlays

They consist of plastic foil and are used for printed circuit boards. Line connections and components are marked on them. Holes are provided on soldering points to identify the measuring point on the conductor side of the printed circuit board more quickly and better.

• Testing PCB
are printed circuits boards to be only used for testing purposes of subassemblies.

• Circuit extracts
are prepared for intricate faults or missing documents.

• Service questionnaire
is used for trouble shooting outside the workshop. Faults are localized by its evaluation.

Safety regulations

It is very important to observe the safety regulations for trouble shooting with subassemblies as the alive parts are not protected against immediate access.

Technological conditions

– Production shop
By testing of all functions of subassemblies each fault is detected and can be removed.

– Repair shop
There are good prerequisites for efficient trouble shooting.

– Field service
is provided for less complicated faults.
Efforts for shooting intricate faults would be too great (transportation and possibilities for use of measuring equipment and tools).

– Equipment of workplaces
in line with the subassembly to be repaired.

Measuring tools are to be arranged in a semicircle and partly on top each other at the workplace.

Tools must be ready to hand at the workplace or, if rarely used, in the drawer.

The workplace must accomodate

• hand tools
• measuring tools
• service documents
• the subassembly to be repaired
• spare parts
• auxiliaries (lubricants, oils, solvents)
• test cords, case for defective components.

2.2. Kinds of faults

For the kinds of faults it is important to know the respective effects of faults.

They are included in table 16.

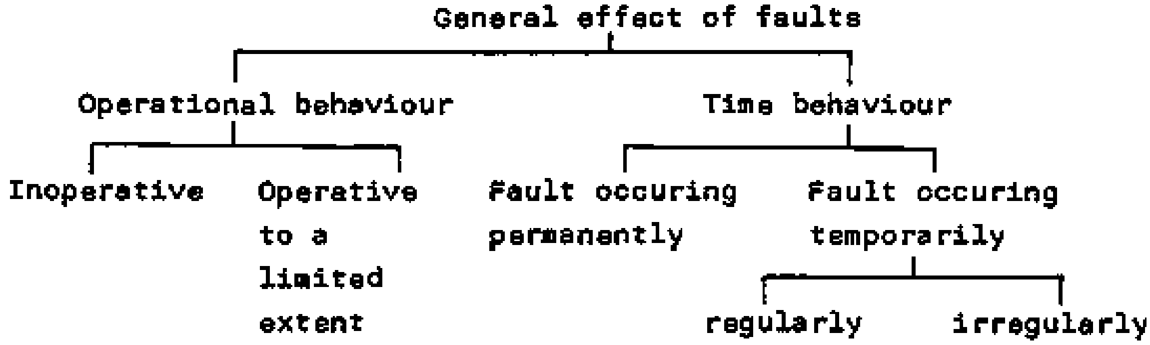


Table 16 General effects of faults

2.2.1. Basic circuit faults

A change of the circuit resistance R_{SN}/Z_{SN} is a basic fault. Z_{SN}/R_{SN} are resistances of the entire circuit at normal operation.

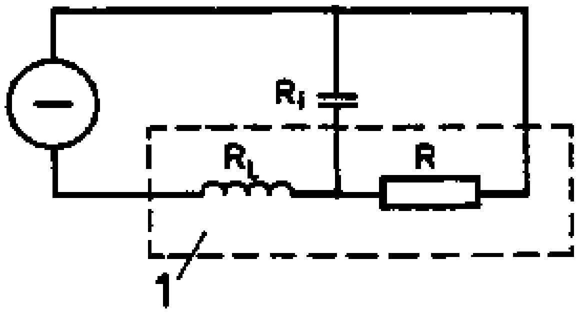


Figure 165 D.C. circuit

1 resistance R_{SN} of faultless circuit

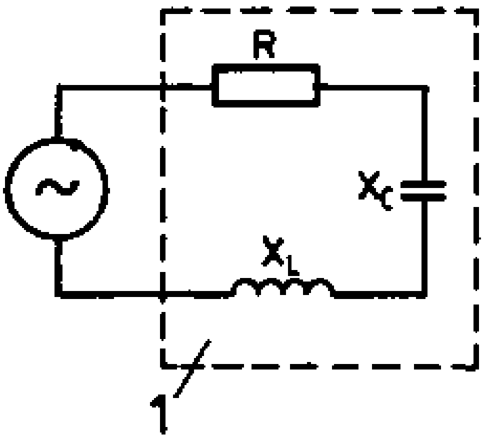


Figure 166 A.C. circuit

1 resistance Z_{SN} of faultless circuit

The basic faults in a D.C. circuit (according to Figure 165) are included in table 17.

Table 17 Basic faults in a D.C. circuit (acc. to Figure 165)

Kind of defect in the circuit	Defective component	Defect on the component

No current flow	Resistor	Interruption between cap and resistive film	R – ?
		Interruption of resistive film	
	Coil	Interruption of winding	R_L – ?
Insufficient current flow	Resistor	Excessive transition resistance cap – resistive film (bad contact making)	
		Too high resistance of resistive film because of aging	
Short circuit	Coil	Interturn short circuit (short–circuit in the D.C. circuit only when normally	
		$R_L >> R$)	R_L ? 0
	Capacitor	Short circuit between capacitor plates (short circuit in the D.C. circuit only when normally	
		$R_L << R$)	R_1 ? 0
Excessive current flow	Coil	Interturn short circuit	
	Capacitor	Fine short circuit between capacitor plates	

2.2.2. Subassembly faults

As to subassemblies there are differences between analogous functional units, such as

– amplifier units
– generator units
– power supply units as well as digital functional units, such as
– switch units
– memory units

Amplifier units

They, essentially, consist of transistors as well as input and output networks.

The faults, which may occur, are mainly:

– No or insufficient amplification
– Distortions of transferred signals

Measuring instruments: Ammeter and voltmeter, measuring generator, oscilloscope.

Generator units

They, mainly, consist of transistors, output networks and feedback networks. The faults, which may occur, are mainly:

– No oscillation or with wrong frequency
– Distorted output signal
– Insufficient oscillation amplitude

Measuring instruments: ammeter and voltmeter oscilloscope, frequency meter

Power supply units

They, mainly, consist of transformers, rectifiers, Z–diodes, electrolytic capacitors, fuse links and resistors (heavy–duty). Faults in the power supply unit mostly result in failure of the entire subassembly, instrument or equipment and can, therefore, be easily localized. The faults, which may occur, are mainly:

– Bad filtering (faulty electrolytic capacitor)

– Voltage too low (charging capacitor has capacitance loss, rectifier aged, transformer has interturn short–circuit).

Measuring instruments: Ammeter and voltmeter

Switch units

They, mainly, consist of transistors as well as input and output networks.

The faults are mostly:

– No switching effected, output level within "prohibited range"
– Wrong threshold level
– Switching time too long

Measuring instruments: Ammeter and voltmeter, logic tester, timer (electronic), oscilloscope (often memory oscilloscope), pulse generator.

Memory units

They, mostly, consist of transistors, diodes and resistors. The following faults are mainly:

– No or undefined switching
– Stable in one position only
– Switching time too long
– Output level withing "prohibited range"

Measuring instruments: See "Switch units".

2.2.3. Component faults

In many cases defective components are not directly determined but by logical conclusion due to a wrong voltage, and wrong current or signal path.

Sometimes measured values permit other interpretations. Therefore, it is recommended to directly check the presumably defective component.

Resistors

Kinds of faults:

– Damage by mechanic al influence (breakage of seramic package)
– Cap faults (interruption, excessive transition resistance)
– Damage by excessive current flow (resistive film burned)
– Damage by spark–over from coil to coil
– Aging of resistive film (excessive resistance value)

Measuring instruments: Ohmmeter, ammeter and voltmeter. The resistance value is mathematically determined by the equation

$$R = \frac{U}{I}.$$

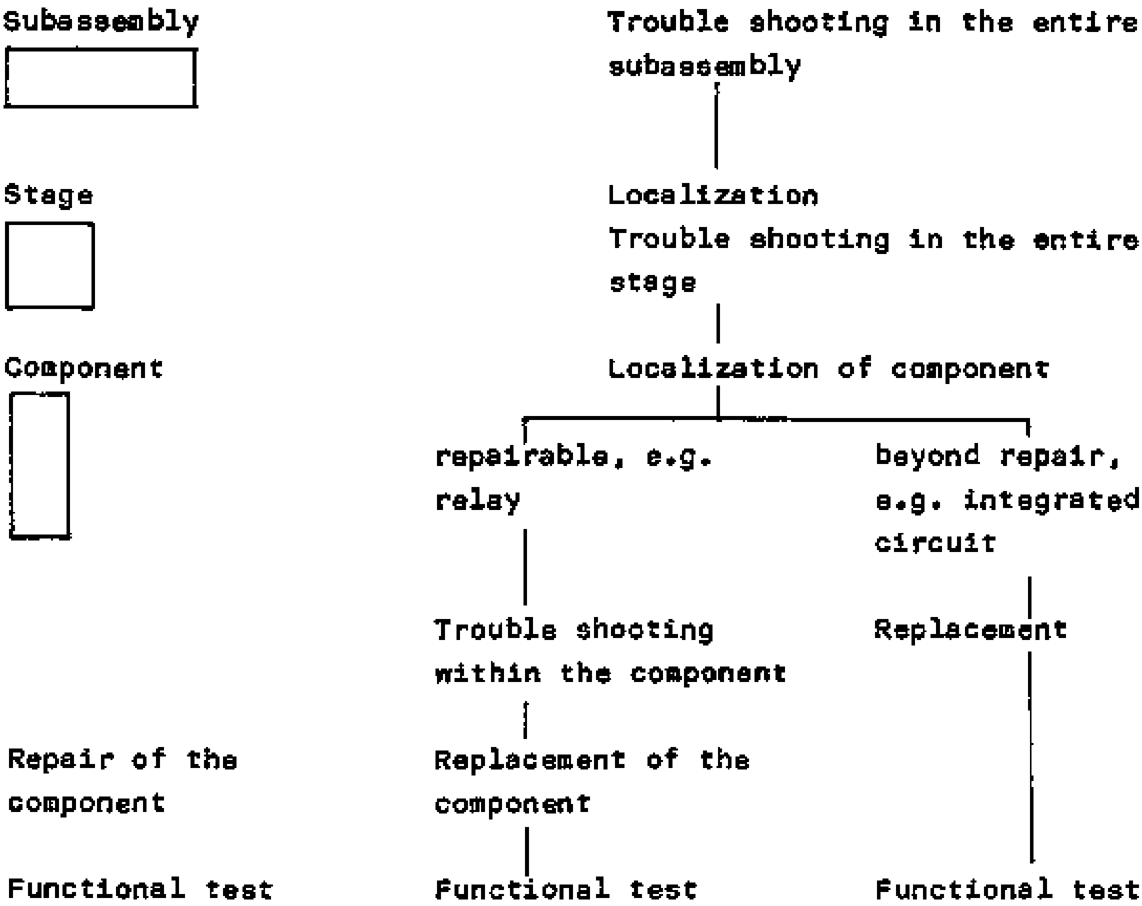


Table 18 Step–by–step localization of faults

Capacitors

Kinds of faults:

- Short circuit
- Decrease of insulation resistance
- Capacitance loss

Measuring instruments: Capacitance meter, ohmmeter for measuring the insulation resistance, ammeter for measuring the residual current.

Capacitors to be unsoldered from the circuit (especially in power supply modules) must be discharged via a resistor first.

Coils

Kinds of faults:

- Interturn short circuit by defective insulation.
- Interruption, especially of thin coil wires, by increased current flow.

Measuring instruments: Inductometer, ohmmeter to determine the interruption, interturn short–circuit tester.

Transistors

Kinds of faults:

- Interruption
- Short circuit
- Excessive collector residual current
- Distorted characteristic

Measuring instruments: Ohmmeter for short circuit and interruption, transistor tester for measuring the collector resisudal current, h−parameters.

Diodes

Kinds of faults:

– Short circuit
– Interruption
– Distorted characteristic

Measuring instruments: Ohmmeter (the measuring voltage applied from ohmmeter to the diode must be lower than the maximum blocking voltage of the diode), diode tester.

Integrated circuits

Kinds of faults:

A wide variety according to the special function of the circuits

– in analogous circuits: crystal" structures destroyed by thermal overload

– in MOS circuits: destruction of crystal structures by inadmissibly high field strength at the inputs.

Measuring instruments: Complex measuring and testing devices (circuit tester)

Contact components

Kinds of faults:

– Interruption
– Excessive transition resistance by contamination, oxidation
– Decrease of spring pressure
– Short circuit
– Loose contact
– Deformed or broken insulating parts
– Wear through of noble metal coat at the contact point

Measuring instrument: ohmmeter

Printed circuit boards

Kinds of faults:

– Track break
– Faulty soldering joints

2.3. Systematics of efficient trouble shooting

2.3.1. Definitions and requirements

The objective is to save time and use less testing and measuring instruments as well as highly qualified staff. Stepwise localization of the fault and pin−pointed testing and measuring based on logical considerations should be the method of working. To prepare this, a thorough information of the form of occurrence of the fault and the preparation of the working place are necessary. The trouble shooting should be started with an inspection in the dead state, followed by putting into operation.

If there is no information of the form of occurrence of the fault, the functional test is to be made.

After putting into operation the subassembly must be carefully inspected to interrupt, in case of emergency, the circuit immediately to avoid further damage. The trouble shooting method is determined by the mechanic depending on the specific technical features of the subassembly, on the kind of fault and on the possibilities of testing and measuring.

2.3.2. Fault inspection

No equipment is required for it. The inspection must be made before any trouble shooting is carried out. The objective of fault inspection is to detect the fault and to get a general impression of the general state of the subassembly (possibly detection of other faults). In this case, time saving is an advantage over other methods of trouble shooting.

For preparation, it is necessary to remove easily mounted parts of cases, screening plates etc. and to clean the subassemblies from contamination, oil or chemical residues.

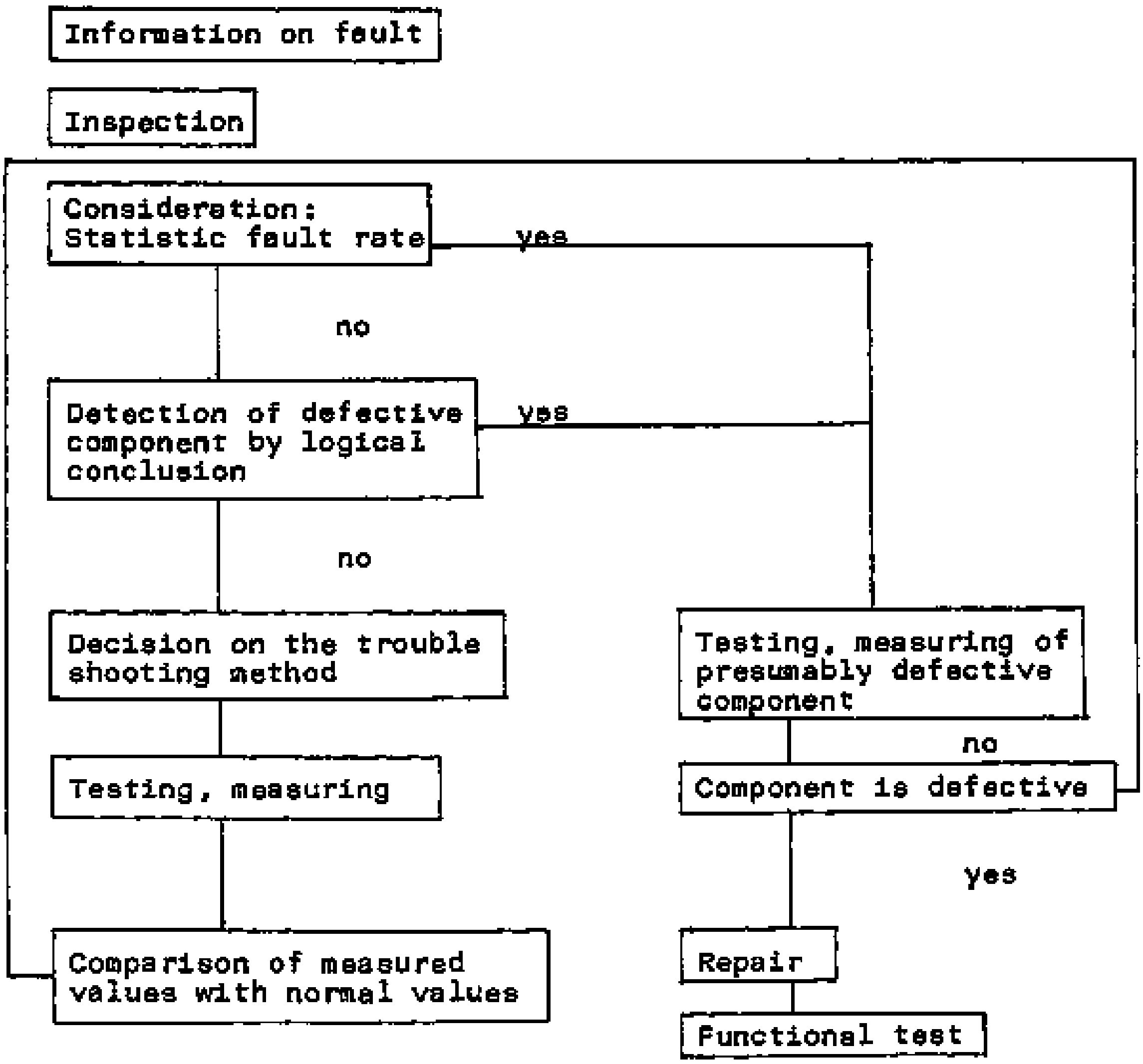


Table 19 Schematic of systematic trouble shooting

Fault detection

The below−mentioned forms of occurence of faults may be of importance for the detection of faults:

Optical perception

Displacement of mechanical and electrical components, chassis, housings and wirings; scorched components and wirings; torn wirings; broken components; chemical decomposition of components and wiring; smoke development of current−carrying components; sparks and high−voltage spark−over; image efects on video displays.

Audible perception

Incorrect noises of mechanically moved parts, such as switches, motors and transfer elements; incorrect signals of subassemblies with electroacoustical transducers; high−voltage spark−over.

Smell

Scorched components and wirings; chemical decomposition of components which develop gases of intense smell; smell of burned oil of overheated bearings.

Perception by contact

Inadmissibly high backlash or incorrect mounting of mechanical transfer elements, switches, operating elements etc.; excessive surface temperature of components, i.e. transistors.

Table 20 Working order of the subassembly during trouble shooting

Working order of the subassembly	Fault detection (perception)			
	optical	audible	by smell	by contact
In operation	yes	yes	b	no
Out of operation	yes	a	yes	yes

a rarely, e.g. defective switches
b sometimes possible but only for a short time

2.3.3. Theoretical fault analysis

The more careful and well−considered the occurrence of fault is analyzed, the more efficient the fault detection.

The theoretical fault analysis is an essential part of fault detection and correlates constantly with the practical fault detection.

The objective is to detect or localize the fault by consideration by means of service documents.

To prepare this, detailed information on the form of occurrence of the fault as well as the study of service documents and technical literature are necessary.

Fault analysis includes the following measures:

Statistic fault rate

Existing empirical values are the basis.

Did the same fault already occur with previous repairs and which component was defect?

Possibly existing fault analyses in writing or notes in the service documents must be included in the analysis.

Logical conclusions

Figure 167 shows an example. The defective component can be gathered from the kind of fault.

The ratio of sizes of the components in the circuit is especially to be taken into consideration.

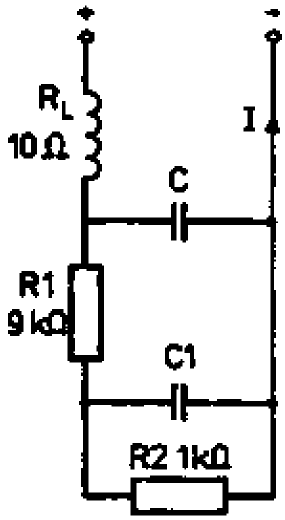


Figure 167 Network

R1 is decisive for current I

For example:

– Fault $I_{actual} >> I_{normal}$.

– Because of the low percentage of the total resistance, an interturn short circuit of the coil is impossible.

– R1 represents 90% of the total resistance of the circuit, a short circuit of C 1 would have an insignificant effect only.

– Result: Short circuit of capacitor C causing a considerable increase of current I.

Determination of the trouble shooting method

Based on the occurrence of the fault and on the knowledge of the function and construction of the subassembly, the methods and the start of trouble shooting are determined. It is to be considered what measuring results are to be expected at normal operation.

Required tools and measuring devices must be at hand. For the practical trouble shooting the mechanic must know the necessary safety regulations.

Evaluation of measuring results

Results are compared with normal values and are the basis of further considerations. Faults localized by logical conclusions make the trouble shooting more efficient. The time of trouble shooting is decreasing with increasing experience.

2.4. Trouble shooting on analogue circuits

2.4.1. Definitions and requirements

Analogue circuits are interconnected stages the inputs and outputs of which are more or less constant, i.e. amplifiers, generators.

The objective of trouble shooting is to localize the fault down to the component or part of the circuit which is not repairable, e.g. transistor array, low−frequency amplifier IC.

Trouble shooting methods are basically used

– to check the circuit in static state. This is based on the circuit diagram.

– to check the circuit in dynamic state. The basis is the circuit diagram and, for complicated and extensive circuits, the general wiring diagram.

2.4.2. Measuring and testing instruments

According to the object and quantity to be measured, the following measuring and testing instruments are used:

Multirange meter

for measuring the static currents and voltages within the subassembly. It is the simpliest and mostly used measuring instrument for trouble shooting in analogous subassemblies.

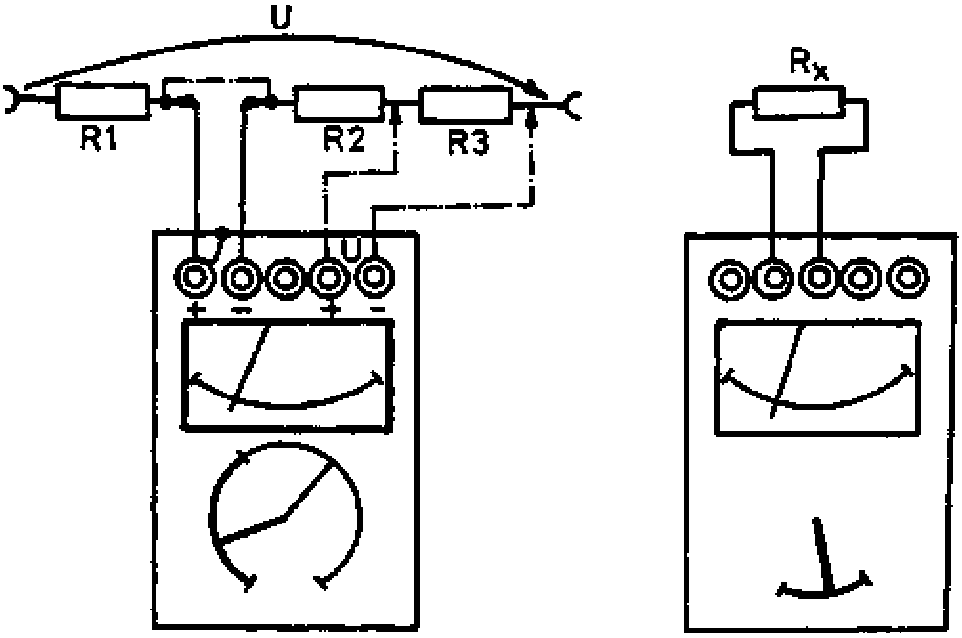


Figure 168 Use of a multirange meter for measuring currents, voltages and resistances

Figure 168 shows measuring circuits which can be applied for measuring in direct–current circuits by means of a multirange meter.

Multirange meters are available for direct and alternating current quantities. Instructions for use:

– To make sure horizontal position in use;

– to avoid unequal heating (e.g. by means of working place lighting);

– to take into account class accuracy (1.0 ... 2.5);

– to check zero position of pointer or to zero the pointer before measuring and in currentless state;

– always to keep the battery area closed since battery connecting terminals may have a high voltage against the earth potential during measuring according to the quantity to be measured;

– to zero the pointer in the respective resistance measuring range before measuring.

Disadvantages compared with electronic measuring devices: Load on measuring point with the input resistance of the multirange meter (up to max. 100 k?V). As to A.C. quantities, measurements are only possible with extremely limited frequency range and, in some cases, limited to sinusoidal quantities as well as average value measurements.

Electronic multirange instruments

are used for the measurement of currents and voltages with high frequency and peak values.

The measurement is made with a very low load on the measuring point. Instruments with digital indication must be used for measurements with high accuracies.

(The basic inaccuracy of a digital display is +/– 1 digit of the "indicated value. Example: 2.734 V is indicated; thus, the inaccuracy of the indicated value is at least +/– 0.001 V).

Measuring generators
for sinusoidal and pulse shaped quantities; for the drive of the subassembly and, especially, for signal tracing and balance work.

Power supply units
for making available the supply voltage of the subassembly.

Oscilloscope
for representation of the curve of a signal in the individual stages and for determination of amplitude and frequencies or time duration of the quantity to be measured. The simplest method is the service oscilloscope.

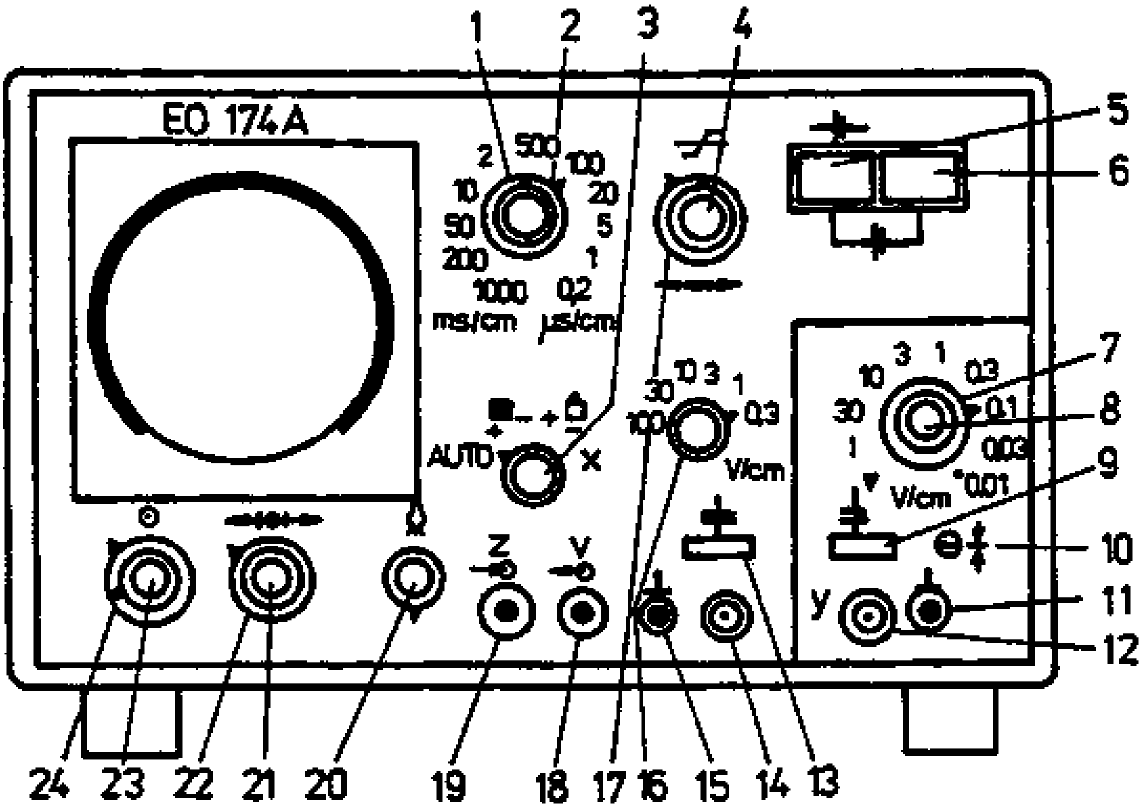


Figure 169 Service oscilloscope (example)

1 $\text{sweep}_{\text{coarse}}$,
2 $\text{sweep}_{\text{fine}}$,
3 trigger selection,
4 trigger level,
5 battery,
6 mains,
7 y divider,
8 y amplitude,
9 key pressed = y input through capacitor,
10 y–0 correction,
11 mass,
12 y input,

13 key pressed = x input through capacitor,
14 x input,
15 masses,
16 x divider,
17 x amplitude,
18 sweep output,
19 z modulation input,
20 scanning illumination,
21 vertical displacement,
22 horizontal displacement,
23 brightness,
24 sharpness

Complex measuring devices
for example, sweep–level measuring sets, selectographs for the representation of transmission curves of selective amplifiers and for balance work.

Resistance measuring instruments
for continuity tests and short–circuit tests and resistance measurements.

L–, C–measuring instruments
for fault detection on components.

Frequency meter
for trouble shooting on generator subassemblies or for setting of the generator frequency.

2.4.3. Fault detection on basic analogous subassemblies

Amplifier

Figure 170 shows a pnp–transistor in an emitter circuit.

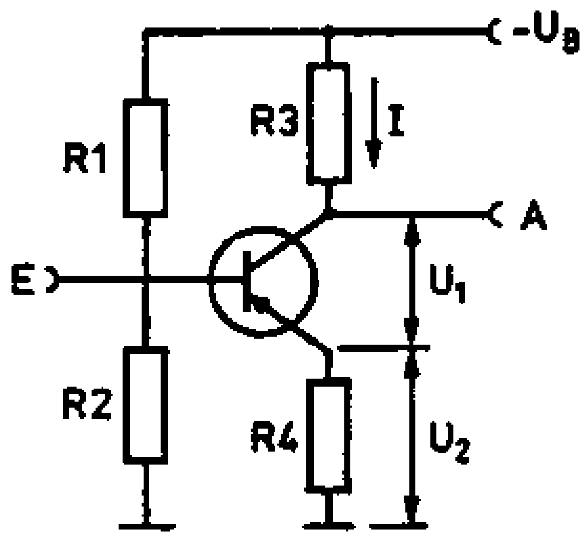


Figure 170 Transistor amplifying stage

Table 21 shows the possible fault effects of given causes of faults.

Table 21 Comparison of causes and effects of faults

Cause of fault	Fault effect		
	U_1	U_2	I

Interruption R 1	–	+	+
Interruption R 2	++	–	–
Interruption R 3	0	++	0
Interruption R 4	0	0	0
Interruption of supply line to the base	+	–	–

+ measured value too high;
– measured value too low;
0 measured value is zero.

When concluding the possible cause of a fault from the fault effect, the change of the current conditions in the transistor amplifier stage, in the event a defect of a component suddenly occurs, must be taken into account.

Operational amplifier

The operational amplifier is the basic stage of many modern circuits. The functional test is made with suitable special testers.

Parameters to be tested are:

– offset voltage
– offset current
– open–loop voltage gain
– operating current

2.4.4. Static trouble shooting methods

Continuity test or short–circuit test

It is used to detect interruptions and short circuits, above all, in low–resistive circuits.

Short circuit: Good possibility for trouble shooting in branched circuits.

Interruption: Good possibility for trouble shooting in meshed circuits.

This method results only in the statement: Short circuit or interruption yes or no.

Preconditions are:

– It is not allowed to put the subassembly into operation.
– Trouble shooting is made in dead state.

Measuring instruments:

– Continuity tester
– Simple ohmmeter

Figure 171 shows an example of a continuity test.

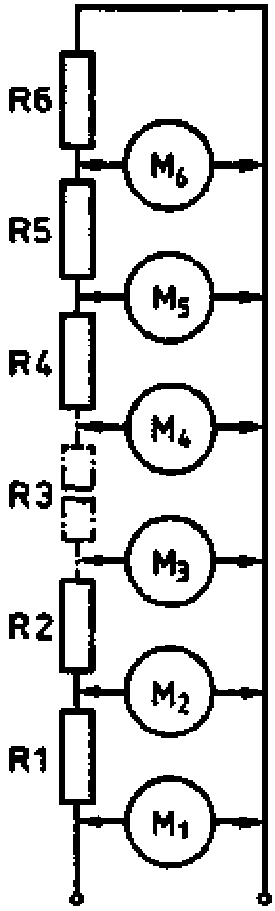


Figure 171 Continuity test

The test is evaluated on the basis: continuity yes (+)/no(–).

Three versions are possible, of which version 3 represents a very efficient method for series connections. The first test value is decisive for the direction of the series connection in which the test is to be continued.

Table 22 Versions of evaluation

Version 1	**Version 2**	**Version 3**
M1 –	M6 +	M4 +
M2 –	M5 +	M3 –
M3 –	M4 +	
M4 +	M3 –	

Figure 172 shows an example of a short–circuit test.

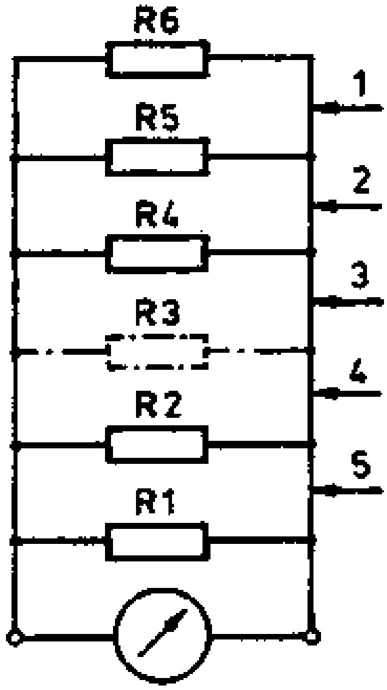


Figure 172 Short−circuit test

The test is evaluated on the basis: short circuit yes/no. The points 1 to 5 are successively interrupted.

A continuity tester is connected to the output terminals.

Should the deflection, when disconnecting an ingoing line, be considerably less (more resistive), the component connected to the point placed before is short−circuited.

Precondition: The continuity tester must not indicate nearly 0 ? at normal function of circuit.

Similar to the continuity test, the short−circuit test can be carried out in three versions.

Voltage measurement

is an often used shooting method since it is not necessary to subdivide the circuit for incorporating a voltmeter.

It is applied in meshed circuits, especially for the measurement of voltages which appear on the individual components upon putting into operation of the subassembly.

Preconditions are:

– It must be possible to put the subassemblies into operation without danger of further destruction of components.

– A signal is not necessary unless certain voltages are switched−on and adjusted by signals.

Measuring instruments:

– High−resistive voltameters for high−resistive circuits.

– Instruments with precision indication, digital voltmeters for measuring close−tolerance voltage levels.

– Multirange instruments

This is made by checking the voltages which must apply to components for setting the bias points. In electronic subassemblies they are mostly D.C. voltages. According to the circuit diagram, the voltage level to be expected is estimated or read before measurement. In the event, the measured value differs from the value to be expected at normal operation of the subassembly, so it must be taken into consideration which component or stage could cause such a change of the voltage level.

Current measurement

This method cannot always be efficiently used. The circuit must be subdivided for the measurement which is problematic with printed circuit boards.

It is applied to

– transistor stages as set current values are of importance;
– power stages for determining the power input;
– power supply stages.

Preconditions are similar to voltage measurement.

When the circuit is subdivided, the subassembly must be put out of operation (danger of destruction of components due to changed bias point; safety regulations to be observed).

Measuring instruments:

– Ammeters (extremely low–resistance ammeters must be applied for low–resistance circuits).

– Precision indicators for values of close tolerance.

– Galvanometers for very low values.

The current measurement is made similar to voltage measurement.

Resistance measurement

This is used for checking of defective components where subassemblies, due to local conditions, such as danger of destruction of other components, cannot be put into operation.

The precondition is that the subassembly must be in a dead state. Measuring instruments:

– Ohmmeters
– Insulation testers

It is performed similar to continuity tests or short–circuit tests, however, with precise resistance–measurement results. This can be done in two versions:

Version 1: Measurement of the resistance of a circuit. If the correct resistance value cannot be estimated, various components must be possibly disconnected. This method is only possible for simple subassemblies.

Version 2: Individual components, e.g. resistors, are separated from the circuit on one side and their resistance value is measured. The resistor may, if required, remain within the circuit during the measurement provided the value of resistance is much lower than the resistance value of the entire circuit.

2.4.5. Dynamic trouble shooting methods

This is applied in subassemblies where the signal has to pass several stages. It is the mostly used method for checking the overall function of a subassembly.

The precondition is that the subassembly is in operating condition:

– Signal transmitters, such as generators, level generators etc.;
– Measuring instruments, such as oscilloscopes, level measuring instruments etc.;
– Sound and image converters etc.

The following methods are applied

- stage−by−stage signal feed and
- stage−by−stage signal measurement.

It is possible to localize the fault stage but it is impossible to detect the defective component.

Stage−by−stage signal feed

This is used if there is no inadmissible load on the input of the individual stage by the signal transmitter.

Figure 173 shows the principle of that method.

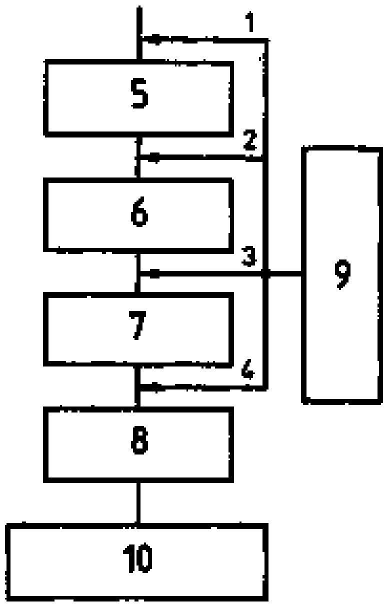


Figure 173 Principle of stage−by−stage signal feed

1, 2, 3, 4 sequences of measurement,
5 stage 1,
6 stage 2.
7 stage 3,
8 stage 4,
9 signal transmitter,
10 measuring instrument

Sequence of measurement: 1 − 2 − 3 or 4 − 3 − 2 or 3 − 2.

In all three cases the stage 2 is detected as defective. A separation is to be made between the stages, if required.

Required input values for individual stages and parameters of stages must be known.

Based on these values it must be considered or gathered from technical documentation which output value the subassembly must have for proper functioning of the subsequent stages.

Stage−by−stage signal measurement

Figure 174 shows the principle. This method is widely used since, in most cases, it is more easier to connect the measuring instrument between two stages than a signal transmitter. Possible sequences of measurement as well as necessary knowledge of the subassembly correspond to those of stage−by−stage signal feed.

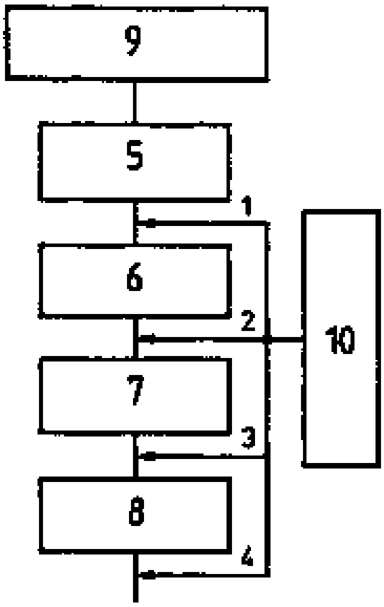


Figure 174 Principle of stage−by−stage signal measurement

1, 2, 3, 4 sequences of measurement,
5 stage 1,
6 stage 2,
7 stage 3,
8 stage 4,
9 signal transmitter,
10 measuring instrument

Example of a trouble shooting

Figure 175 shows the construction of a two−stage RC−amplifier. Figure 176 shows the general wiring diagram. The check of the output signal with an oscilloscope showed a too low amplification compared with the specification for the subassembly mentioned by the manufacturer.

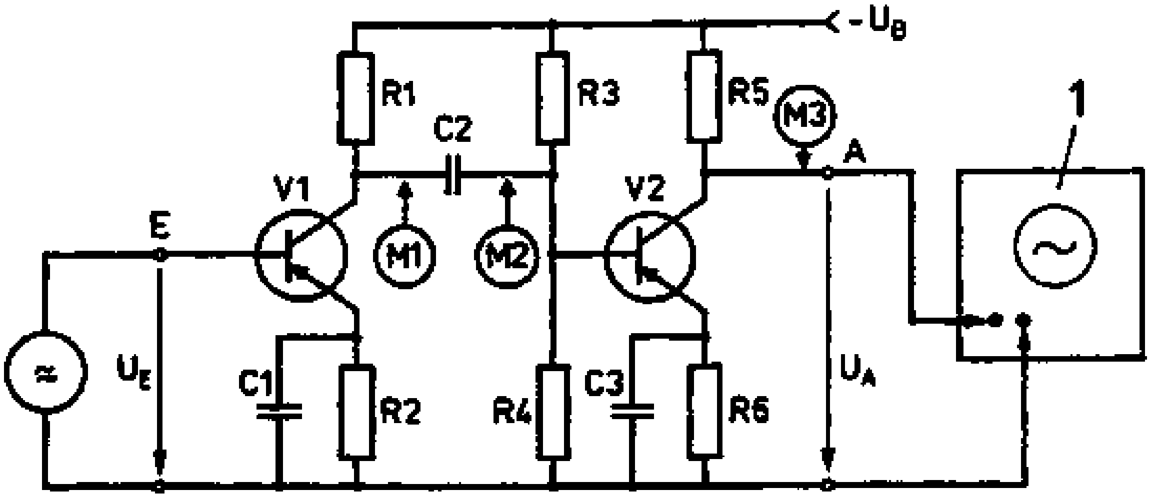


Figure 175 Two−stage RC−amplifier

M1, M2, M3 measuring points of the oscilloscope. 1 oscilloscope

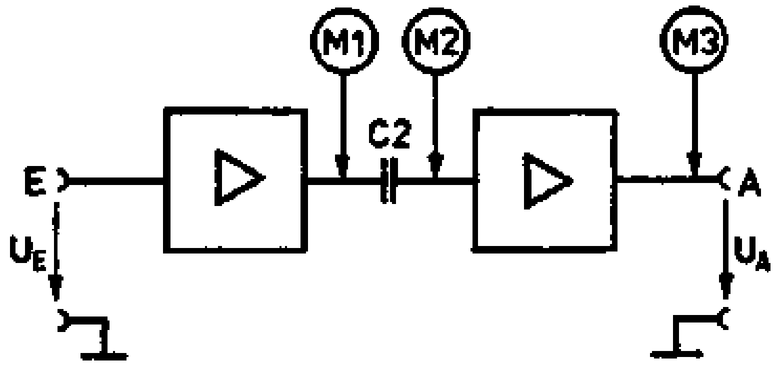


Figure 176 General wiring diagram of the RC−amplifier

values: U_{SSE} = 1 mV, U_{SSM1} = 25 mV, U_{SSM2} = 2 mV, U_{SSM3} = 50 mV

Checking the signals at the points MI and M2, it was sure, that the amplifier stages 1 and 2 have a sufficient amplification. The level drop between MI and M2 is inadmissible. C 2 is a coupling capacitor where an imperceptible voltage drop is admissible only.

Conclusion: C 2 defective!

The capacitance loss of C 2 can be proved by a capacitance meter. (In order to state the full functional reliability of the subassembly ace. to Figure 175, further testing procedures are necessary, e.g. testing the loss of amplification as a function of the frequency).

<u>Testing sets for complex functional test</u>

For several trouble shooting and testing work special tasting sets must be set up, particularly for the

− functional tests to detect the faults,
− fault localization.
− alignment work.

Figure 177 shows a sweep−level measuring set−up. It is used for the alignment of selective amplifiers, i.e. for setting the transmission curve shape, e.g. for radio transmitters and receivers.

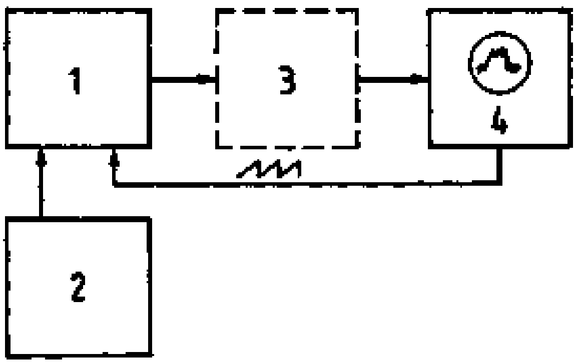


Figure 177 Sweep−level measuring set−up

1 sweep generator (wobbler),
2 high−frequency signal generator,
3 device under test,
4 oscilloscope

This measuring set is also available as complex device (selectograph). The measuring set offers an efficient way of complex testing of the subassembly and immediate fault detection. The faulty stage is localized by stage−by−stage signal feed.

2.5. Trouble shooting an digital circuits

2.5.1. Definition and requirements

Digital circuits are the interconnected stages with logical functions, e.g. inverter, AND−, OR−, NAND−, NOR−elements, triggers and others.

The objective is to localize the fault to the basic logical circuit.

Fundamental methods for trouble shooting are used

– to check the voltage levels H (high) and L (low). The basis is a circuit diagram;

– to check the logical statements 1 and 0. The basis is the logical diagram to Figure 178;

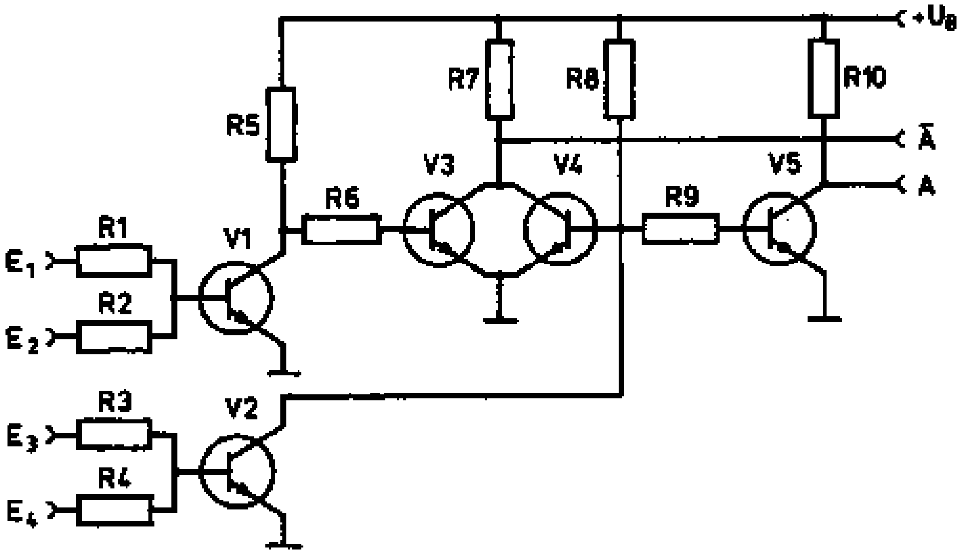


Figure 178 Circuit diagram of a digital circuit with four inputs and one direct output and one negated output

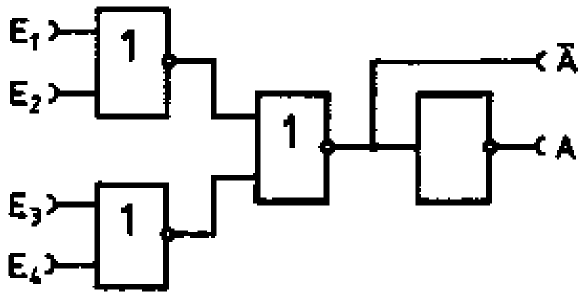


Figure 179 Logic diagram of the digital circuit as per Figure 178

– to perform the dynamic test, for example with clocked control.

2.5.2. Measuring and testing instruments (application)

<u>Multirange instruments</u>
used for measuring the voltage level in the static states H and L and for measuring the supply voltages of stages as well.

<u>Broad−band dual−beam oscilloscopes</u>
used for dynamic tests of circuit state junctions, measurement of propagation delays.

As for single pulses, storage oscilloscopes are required for these measurements. Simple oscilloscopes are also used for static tests of levels H and L (advantage over multirange instruments: inertialess measurement).

Pulse generators
used for single pulses and pulse sequences for the drive of stages.

Power supply units
used to provide the supply voltage to subassemblies or for static drive of stage inputs.

Logic test prods

This is a simple digitally indicating tester for the static check of the logic states 1 and 0 or of the levels H and L and of the "prohibited range".

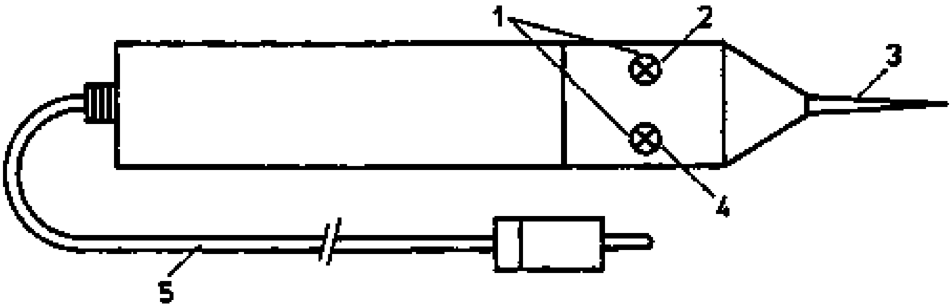


Figure 180 Logic test prod

1 indication for "level in prohibited range",
2 indication for level "L",
3 prod tip,
4 indication for level "H",
5 power supply line

Procedure:

The test point is touched by means of the test prod. The logic state at the test point is evaluated by checking the lamps. Figure 181 shows the correspondence of the levels with the indication on the test prod; for TTL output levels of positive logic. Dynamic states of the circuit (e.g. pulse frequency) can be evaluated to some degree by means of various types of test prods.

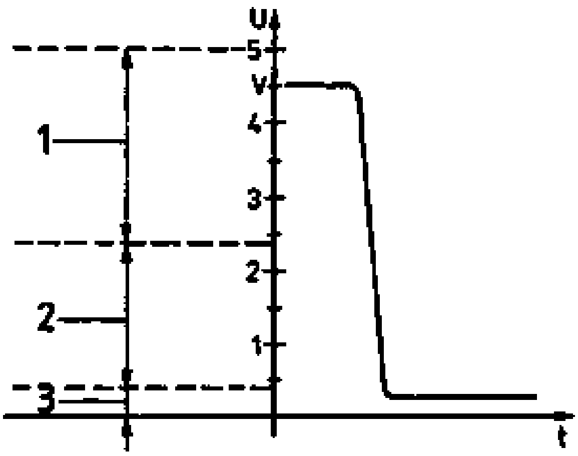


Figure 181 Test prod indication for TTL output level

1 range for level "H" (lamp 4)
2 prohibited range (lamps 2 + 4)
3 range for level "L" (lamp 2)

Logic test keys

These are used for fault determination in integrated circuits for the static states; pulse duration (e.g. duration of H and L pulses for pulse sequences); pulse slot (e.g. time slot of a pulse sequence compared to a reference pulse sequence); pulse polarity (e.g. for initiating pulse sequences). Figure 182 shows a logic test key for TTL circuits.

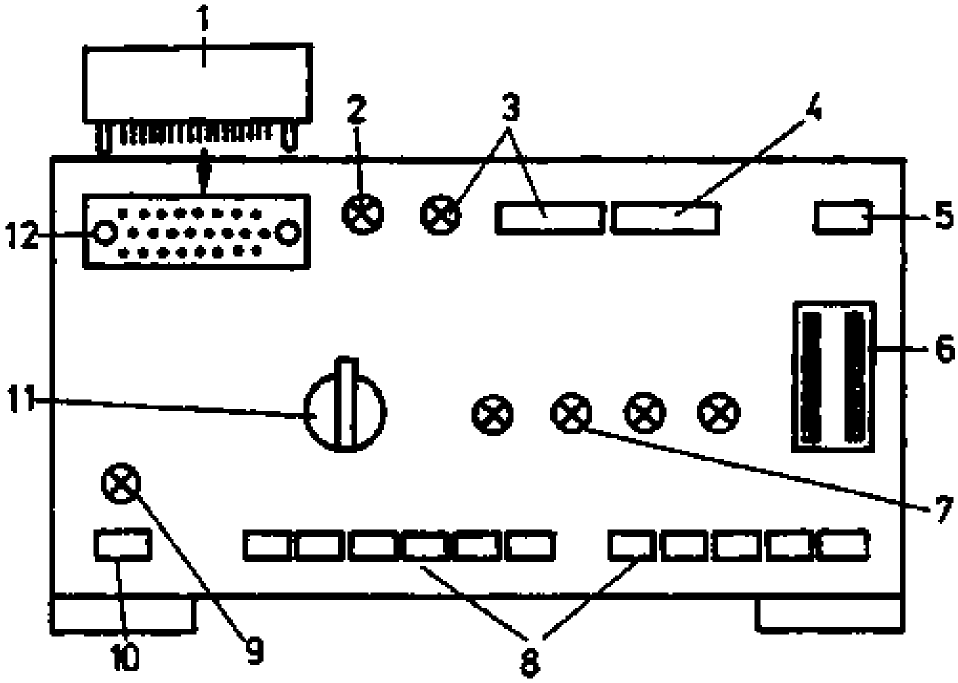


Figure 182 Logic test key for digital integrated circuits

1 programming plug for IC type,
2 lamp for IC,
3 key and lamp to test contact making of IC,
4 key for type selection,
5 key for clock cycle generation,
6 socket for TTL circuits,
7 result read−out,
8 key set for input levels,
9 mains control,
10 mains key,
11 type selector switch,
12 socket board for programming plug.

Procedure:

The type of circuit is set by means of a type selector switch and the IC is plugged into the socket. The circuit is tested after checking the contact making of IC by pressing the key and checking by means of the signal lamp. The circuit pins are driven by pressing the key. Four lamps indicate the respective test result. The test result is evaluated by means of a reference list.

2.5.3. Fault detection on basic digital subassemblies

Inverter

Figure 183 shows an npn transistor in an emitter circuit. Its logic function is $E = \overline{A}$.

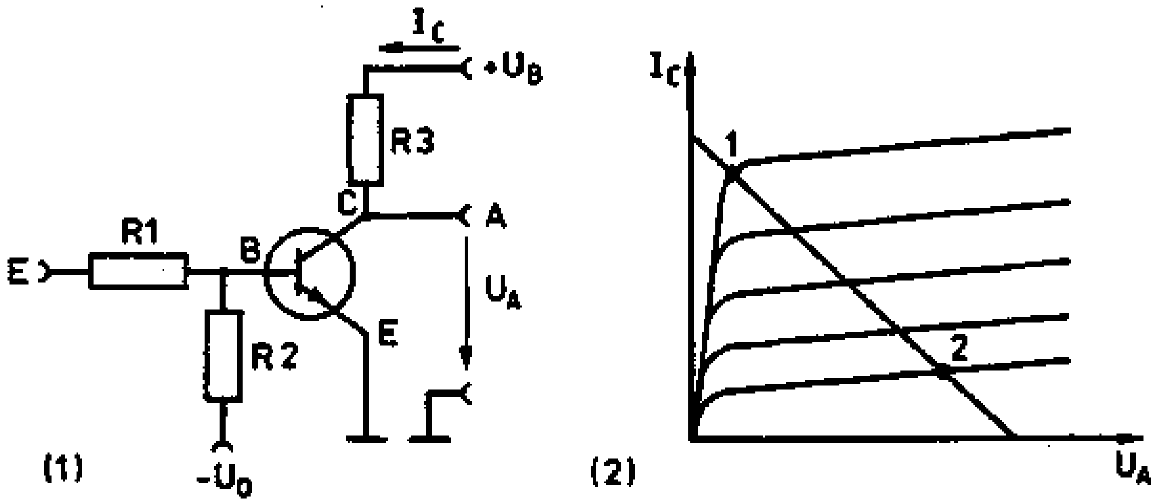


Figure 183 Transistor stage with two statical switching states

(1) current flow,
(2) diagram
1 transistor conductive,
2 transistor blocked

Table 23 shows the change of the output levels for all possible causes of faults of the stage.

Any "cause of faults listed in table 23, with respect to different input levels, effects for A the statement "continuously L" or "continuously H" and is equal to "transistor conductive" or "transistor blocked". These two statements cover most of the faults occuring in digital circuits.

Table 23 Causes of faults on switching stage ace. to Figure 183

Cause of fault	Level at input E	Level at output A
Interruption R1	L	H
	H	H
Interruption R2	L	L
	H	L
Interruption R3	L	L
	H	L
Open−circuit operation B	L	H
	H	H
Open−circuit operation E	L	H
	H	H
Open−circuit operation C	L	H
	H	H
Short circuit B−C	L	L
	H	L
Short circuit B−E	L	H
	H	H

Short circuit E–C	L	L
	H	L
Faultless	L	H
	H	L

The fault detection "continuously H or L" listed in table 23 admits 4 or 5 different interpretations for the cause of the fault. Consequently, testing the logic states at A only permits to limit the causes of faults. The relevant cause of fault can be exactly detected by static current and voltage measurements.

AND–, OR–, NAND–, NOR elements

However, the causes of faults are not basically detectable by static tests of logic levels.

Example: NAND stage according to Figure 184.

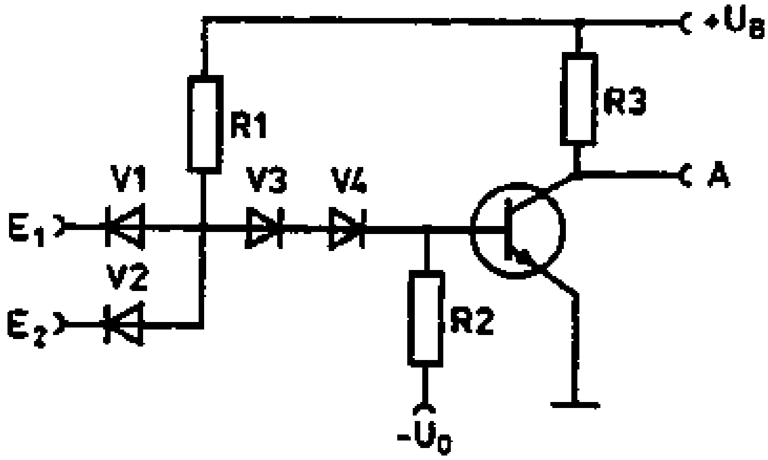


Figure 184 NAND stage for detecting the causes of faults

Table 24 shows the causes of faults of that circuit.

Table 24 Causes of faults on the NAND element ace. to Figure 184

E_1	E_2	Level at output A						
		Faultless	Short circuit at Interruption at					
			R3	R2	R3	V3	V1	V2
L	L	H	H	L	H	L	H	H
L	H	H	H	L	H	L	L	H
H	L	H	H	L	H	L	H	L
H	H	L	H	L	L	L	L	L

It can be seen that a short circuit of V3 shows no effects on the static behaviour. The fault is to be detected by dynamic testing, e.g. switching transient behaviour.

2.5.4. Trouble shooting methods

As to digital circuits, great efforts are necessary for detection of a fault and of the cause of the fault due to the variety of possible combinations of input levels H or L and of the respective output levels.

One point of emphasis in the preparation of trouble shooting is to elaborate efficient test methods.

The objective is to localize the fault to the basic stages (e.g. AND−, OR−, NAND−, NOR elements, inverters and triggers) and to the integrated circuit, respectively.

As to extensive circuits, especially those using large−scale integrated circuits, the replacement of subassemblies (replacement of defective plug−in units) often is the only possible way to remove the fault with justifiable expenditure of time.

<u>Instructions for test work</u>

The testing of logic states also requires the drive of stages (test points) within the circuits. The load on the test points by the testing instruments is to be taken into account. Exceeding of admissible load leads to indefinite states and, thus, to wrong conclusions. As for clock−actuated subassemblies, external clock generators must be connected. The correct timing is to be considered. Before testing, internal memory elements must, basically, be put into a definite initial state.

<u>Test step tables</u>

For digital circuits test step tables can be prepared for input and respective output connections.

Complete test step tables include all possible combinations of input and output interconnections.

Optimum test step tables include all necessary combinations for a full functional test.

At least, four test steps are necessary since only with these four input connections there is always a variable which, because of its change, is in a position to change the output state A.

For sequential circuits the fault is to be detected from the input connections as well as the internal switching states and the respective output connections.

2.6. Automation of test procedures

The necessity results from increasing integration level not only with analogous but also with digital subassemblies. In some cases, trouble shooting is only possible by means of complex functional tests.

Test pieces:

– components (integrated circuits) and
– plug−in units.

Test stands:

– Test stand for IC, manual workplace with "good/bad" automatic statement.
– Test stand for IC, computer−controlled
– Test stand for plug−in units, manual workplace
– Test stand for plug−in units, computer−controlled

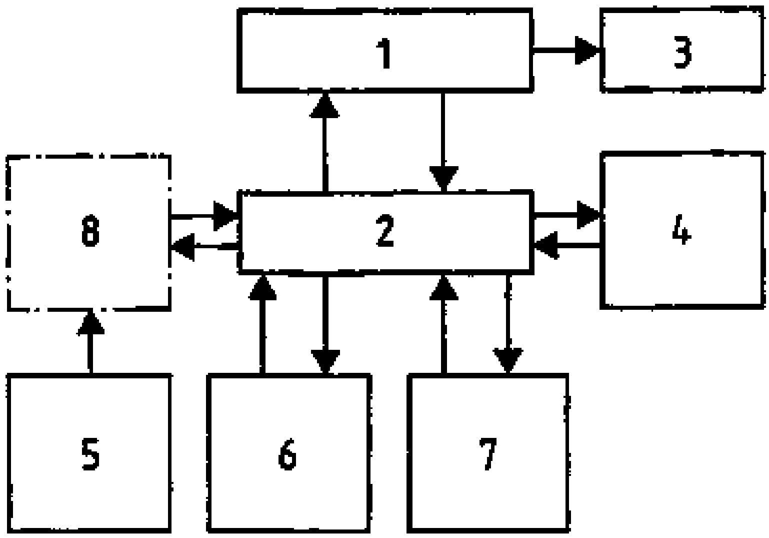


Figure 185 Set−up of a computer−controlled test stand for plug−in units (example)

1 electronic data processing machine,
2 interface,
3 printer,
4 measuring instruments,
5 power supply unit for device under test,
6 plug−in unit load,
7 test generator,
8 device under test (plug−in unit)

The procedure is as follows:

The plug−in unit to be tested is plugged into the holding device.

The test program based on test step sequences is input into the computer (e.g. floppy disks).

In this case, the testing possibilities are:

− Single testing (to be released by the operator), i.e. step−by−step "approaching" to the fault;

− Complex testing, i.e. the test program is completely run or the testing is interrupted in case of occurrence of faults.

The test log is printed by a printer.

2.7. Fault removal

The fault is duly removed when the subassembly has the same use−value properties as before the occurrence of the fault.

The fault removal in modern electronic subassemblies is very complicated because of the use of printed circuit boards and of higher packaging density.

To handling the components, the same conditions apply as to the assembly of electronic subassemblies.

<u>Preparation</u>

− In the event a component must be replaced, the new one must be ready at hand before disassembling the defective component.

− In the event the wirings must be disconnected in order to replace a component, the connections of the individual wires are to be noted depending on the colours of the wire insulation or on other features of the wires. The individual wires can also be marked, if possible.

– The subassembly must be disassembled only to the extent necessary to permit components to be quickly replaced without damaging other parts of the subassembly.

<u>Replacement of components</u>

The replacement is usually made by unsoldering and resoldering the components.

Firstly, the component must be detached from the wiring, then it is removed; the new one is fitted in reverse order.

After replacement of the component the subassembly is to be subjected to a final functional test.

3. Selected basic circuits with subassemblies

3.1. Basic circuits of heavy–current electrical engineering/electronics

In the heavy–current field these units are mostly relatively self–contained parts of an electrical installation with respect to construction, mechanical parts, circuitry or function.

3.1.1. Example 1: thyristor unit

Figure 186 shows a subassembly as smallest functional and constructional unit within a bridge circuit. It comprises all devices directly necessary for operation and protection.

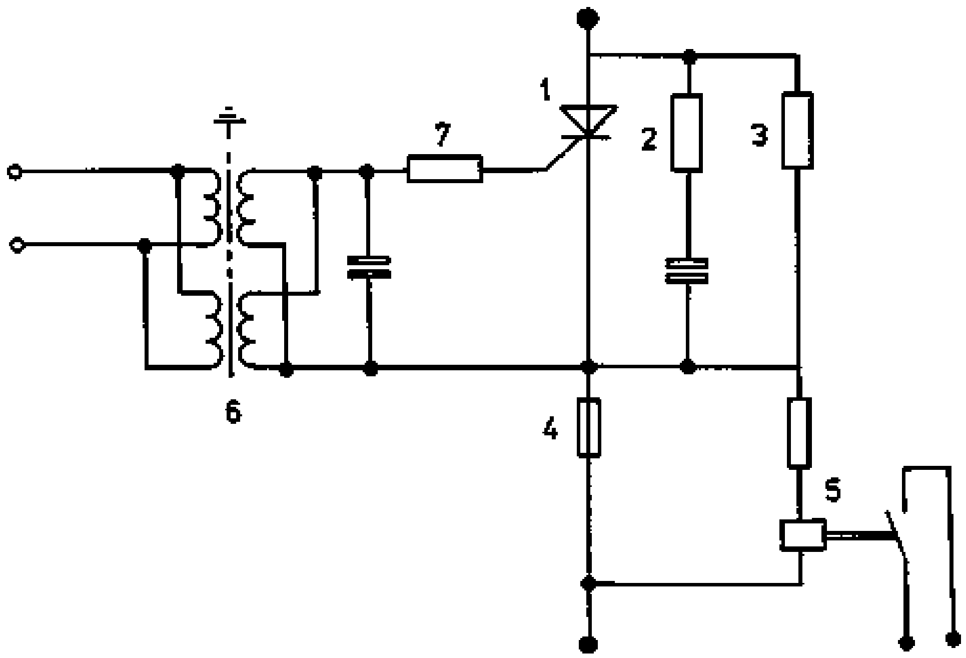


Figure 186 Thyristor unit

1 thyristor,
2 carrier wiring,
3 balancing resistor for series connection,
4 high–speed fuse,
5 signal relay for fuse supervision,
6 pulse transformer,
7 limiting resistor

3.1.2. Example 2: voltage multiplier circuit

Figure 187 (1) shows a multiplier circuit where the capacitor C1 is charged from u to $\sqrt{2} \cdot u$, by the negative half−wave through the diode V1. The positive half−wave, in series with the voltage through C1, charges C2 through V2 to $V = 2\sqrt{2} \cdot u$ The circuit can be extended.

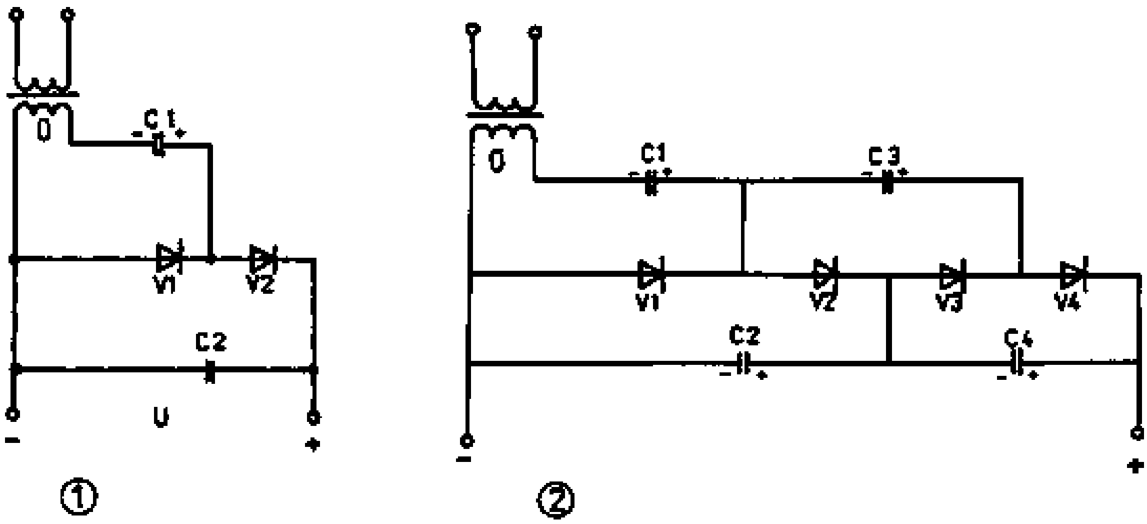


Figure 187 Voltage multiplication

(1) doubler circuit,
(2) quadrupler circuit

Figure 187(2) illustrates multiplication of the voltage at the rectifier side of the transformer. Once C2 is charged to $2\sqrt{2} \cdot u$, C3 is charged to the same voltage through C2, V3 and C1.

C1, C3 and the output voltage at the rectifier side of the transformer add up to $4\sqrt{2} \cdot u$ which is equally distributed over C2 and C4.

3.2. Basic circuits of information electrical engineering/electronics

In information electrical engineering, arrangements of components belonging together with respect to construction, mechanical parts, circuitry or function, are called "modules".

3.2.1. Example 1: mixing stage with oval gate MOSFET

In addition to decoupling of the input circuit and oscillator circuit, there is little ripple and a small output frequency spectrum. The circuit is widely used, inclusively in VHF engineering. Mixers with field effect transistors have a wide range of modulation and a high resistance to cross modulation. In addition to single−ended and push−pull circuits, multiplication mixers can be relatively easily made.

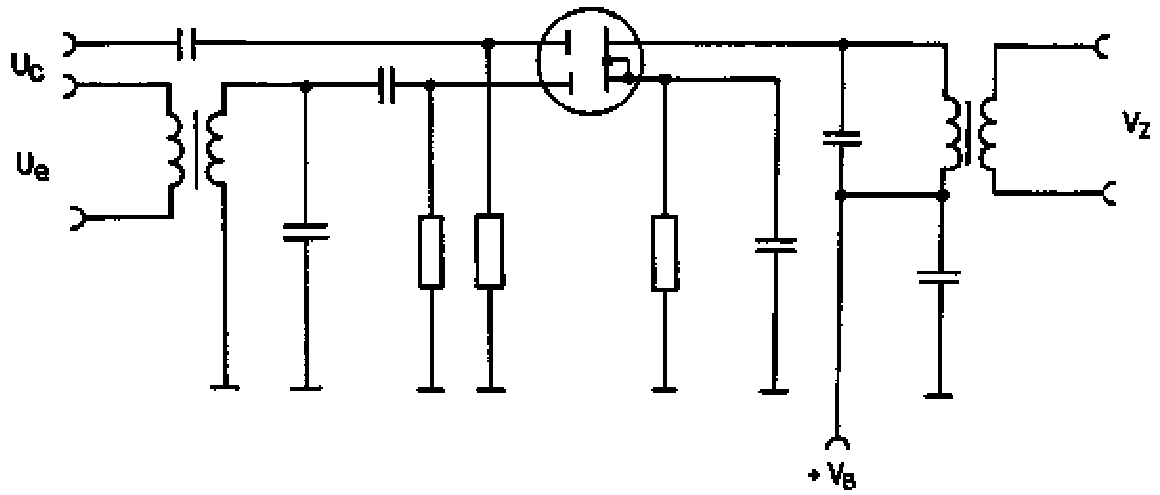


Figure 188 Mixing stage for oval gate MOSFET

3.2.2. Example 2; intermediate–frequency amplifying stage

L1 and C2, C3 form an intermediate–frequency circuit. It can efficiently reduce the damping effect of Rek and the detuning by CS. Such oscillating circuits are well suited for resistance adaptation between resonance and load resistances. The influence of parasitic capacitances is reduced. The transistor output capacitance through CS is in parallel with CKr. Thus the transistor capacitance influences the resonance frequency of the circuit CKr//L2. The capacitance of the transistor depends on the bias point.

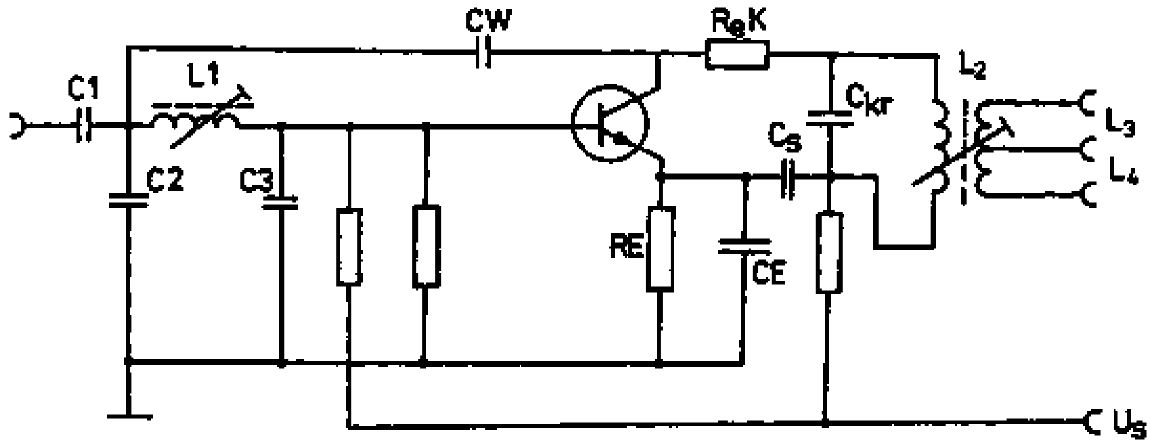


Figure 189 Intermediate–frequency amplifying stage

Questions for recapitulation and testing

1. How is a PCB constructed?

2. What material are PCB made of?

3. What methods are applied for PCB assembly?

4. What does proper manual assembly imply?

5. What are the requirements on soldering of PCB?

6. What does the process of bath soldering imply?

7. What does "wave soldering" mean?

8. What is the difference in quality of the individual methods of rectification?

9. What does the term "filtering" mean and how is filtering achieved technically?

10. What is the specific purpose of switching power supply units?

11. What are amplification and damping?

12. Where is the output of the amplified signal of a transistor? (emitter circuit, collector circuit, base circuit)

13. What is the significance of negative feedback for amplification?

14. What is an operational amplifier?

15. How is power amplification achieved?

16. What are the differences and common features of transformers and converters?

17. How do faults occur in electronic circuits?

18. What knowledge must the trouble shooter have?

19. What facilities are necessary for trouble shooting?

20. What kinds of faults are there?

21. What is the systematic procedure of trouble shooting?

22. What trouble shooting methods are there?

23. What is to be considered for fault removal?